LGA50D Low Profile Series

92.4 Watts
Non Isolated DCDC Converter

Total Power: 92.4 W
Total Current: 50 A(Single)
25 A(Dual)
Output Voltage: 0.6- 3.3 Vdc
# of Outputs: Dual or Single

Special Features

- 2 phase design
- Dual or single output configuration possible.
- Efficiency up to 92% @2.5V, 2 phase
- Small size 1" x 0.51" x 0.24" (LxWxH)
- PMBus^{TM} supporting
- No minimum load requirement
- Wide operating temperature range
- Exceptional power density
- Automatic loop compensation
- Excellent transient response
- Analogue or Digital control
- Tape and reel packaging
- Reflow compatible
- Possible to stack up to 8 phases for 200A
- I-mon and T-mon supported
- Solder bump termination
- IPC9592B compliant @ Vin = 12Vdc

Safety

Designed to meet EN60950-1 and 62368-1

Product Descriptions

The LGA50D power supply features a 7.5 to 14Vdc input voltage range and a 92.4W output power.

The LGA50D is a new design of high performance DC-DC converter. LGA50D has 2 phase design. It offers a total 92.4W output with just dimensions of 1.0"x0.51"x 0.24". State-of the-art circuit topology provides a very high efficiency up to 92% @2.5V 2 phase condition which allows an operating temperature range of -40 ^{O}C to +85 ^{O}C.

Further features include remote On/Off, variable output voltage as well as over-current protection, over-voltage protection, and over-temperature protection.

Applications

This converter has been designed to address a wide range of applications where low-voltage high current power rails are required and with a current density of 98A/Sq-inch, applications where available space is critical, the LGA50D can be used. The output voltage range of 0.6V to 3.3V with adjustable start-up timing and ramp rate covers a multitude of applications from powering the most complex IC's to Led's. The surface mount package is specifically for ease of use in production with termination pins around the outer edges allows easy inspection.

Model Numbers

Model Number	Input Voltage	Output Voltage	Minimum Load	Maximum Load
LGA50D-01DADJLPJ	7.5-14Vdc	0.6-3.3Vdc	0A	50A
LGA50D-01DADJLP1J	7.5-14Vdc	0.6-3.3Vdc	0A	50A

Ordering information

LGA	50	D	-	01	D	ADJ	LP		J
①	②	③		④	⑤	⑥	⑦	⑧	⑨

①	Model series	LGA: Series Name
②	Output current	50: Rated Output Current = 50A
③	Control	D: Digital Control POL
④	Input Voltage Range	01: 7.5 to 14Vdc
⑤	Number of Outputs	D: Dual Output
⑥	Output type	ADJ: Adjustable Output
⑦	Mechanical Options	LP: Low-profile solder bump
⑧	Other Options	Blank: Latching mode during protection 1*: Auto-recovery
⑨	Rohs Compliance	J:Pb free (Rohs 6/6 compliant)

*Current sharing with auto-recovery mode for 1 module only (TBD)

Electrical Specifications

Absolute Maximum Ratings

Stress in excess of those listed in the “Absolute Maximum Ratings” may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply’s reliability.

Table 1. Absolute Maximum Ratings:

Parameter	Model	Symbol	Min	Nom	Max	Unit
Input Voltage (DC continuous operation)	All models	V_{IN}	-	-	15	Vdc
Operating Ambient Temperature[1]	All models	T_A	-40	-	+85	ºC
Storage Temperature	All models	T_{STG}	-40	-	+125	ºC
Output Voltage	All models	V_{out}	0.6	-	3.3	V
Logic I/O voltage SHARE,EN0, EN1, PG0, PG1, SALRT, SCL, SDA, SYNC, VSET0, VSET1,CFG, ADDR, ASCRCFG	All models		-0.3	-	6.0	V
Analog input voltages VS1+, VS1-, VS2+, VS2-	All models		-0.3	-	6.5	V

Note 1 - At low temperatures, (at <-20degC), the accuracy of PMBus™ monitored parameters will be adversely affected.
At high temperatures, please refer to “Thermal Derating” section.

Input Specifications

Table 2. Input Specifications:

Parameter	Conditions[1]	Symbol	Min	Nom	Max	Unit
Operating Input Voltage, DC[2]	$0.6 \le V_O \le 3.3$ V	V_{IN}	7.5	-	14	V
Maximum Input Current	V_{IN}=7.5Vdc	$I_{IN,max}$	-	-	20	A
Standby Input Current (V_O = Off, I_O = 0A)	f_{SW}=615KHz f_{SW}=800KHz	I_{IN}	- -	47 50	52 55	mA mA
Standby Input Power (V_O = Off, I_O = 0A)	f_{SW}=615KHz f_{SW}=800KHz	P_{IN}	- -	0.57 0.60	0.63 0.66	W W
Efficiency at 12V & 25 ^{O}C	1.0V at 50A & 615KHz 1.8V at 44A & 800KHz 2.5V at 34A & 800KHz 3.3V at 28A & 800KHz		84 87.5 89 90	85 88.5 90.5 91.1	- - - -	% % % %
Input Capacitor(Internal)			-	28.2	-	uF
Input Capacitor(External required)[3]			-	132	-	uF
Input Voltage UVLO Threshold Range	Falling		6.5	6.9	-	V
Input Voltage UVLO Threshold Range	Rising		-	7.2	7.5	V
Logic Input/output Characteristics						
Logic Input Low, VIL			-	-	0.8	V
Logic Input High, VIH			2	-	-	V
Logic Output Low, VOL	2mA sinking		-	-	0.5	V
Logic Output High, VOH	2mA sourcing		2.25	-	-	V
Logic Input Leakage Current			-100	-	100	nA

Note 1 - Typical values given at Vin=12V, switching frequency= 615KHz for 0.6V ≤ Vo ≤ 1V and switching frequency =800kHz for 1V < Vo ≤ 3.3V, 25^{O}C , unless otherwise specified under conditions.
Note 2 - To maintain compliance to IPC9592B, input voltage must be kept at ≤ 12V.
Note 3 - Minimum:6 x 22uF/16V 0805 ceramic cap (C2012X6S1C226M125AC or equivalent)

Output Specifications

Table 3. Output Specifications:

Parameter	Conditions	Symbol	Min	Nom	Max	Unit
Output Voltage[2]	V_{IN} = 7.5V to 14V	V_O1, V_O2	0.6	-	3.3	Vdc
Output Current[3] (Independent Output 1 and 2)	V_O1 or V_O2 = 0.6V V_O1 or V_O2 = 1.0V V_O1 or V_O2 = 1.8V V_O1 or V_O2 = 2.5V V_O1 or V_O2 = 3.3V	I_O1 I_O2	0 0 0 0 0	- - - - -	25.0 25.0 22 17.0 14.0	A A A A A
Combined output 1 and 2	Vo = 0.6V Vo = 1.0V Vo = 1.8V Vo = 2.5V Vo = 3.3V	I_O	0 0 0 0 0	- - - - - -	50 50 44 34 28	A A A A A
Output Power	All	Po	-	-	92.4	W
Output Set-point Accuracy[1]	Set by PMBus or 1% trim resistors		-1.2	-	+1.2	%
Output Voltage Set-point Resolution	Set by PMBus™ command	V_O	-0.05	-	+0.05	%
Output Voltage Positive Sensing Bias Current	VS [0,1] + = 4V (negative = sinking)		-100	-	100	μA
Output Voltage Negative Sensing Bias Current	VS [0,1] - = 0V		-	20	-	μA
Line Regulation	0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 3.3V		- -	2 0.2	10 1	mV %
Load Regulation	0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 3.3V		- -	5 0.5	10 1	mV %
Ripple and Noise (with recommended caps) Single Output	0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 3.3V		- -	10 1	20 2	mV_{pk-pk} $\%_{pk-pk}$
Ripple and Noise (with recommended caps) Dual outputs(Vo1, V_O2)	0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 3.3V		- -	10 1	20 2	mV_{pk-pk} $\%_{pk-pk}$
Transient Response Deviation (Independent Output 1 and 2)	50% of I_O step load, slew rate 1A/us 0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 5.0V		- -	50 3	60 4	mV_{pk-pk} $\%_{pk-pk}$
Transient Response Deviation (Combined output 1 and 2)	50% of I_O step load, slew rate 1A/us 0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 5.0V		- -	30 3	40 4	mV_{pk-pk} $\%_{pk-pk}$

Output Specifications

Table 3. Output Specifications, con't:

Parameter	Conditions	Symbol	Min	Nom	Max	Unit
Output Capacitor per Output (external minimum)[3]	Dual outputs	C_O	-	2200	-	uF
	Single output	C_O	-	2400	-	uF
Switching Frequency[5]	0.6V ≤ Vo ≤ 1V		615	615	800	KHz
	1V < Vo ≤ 3.3V		-	800	-	KHz
PMBus™ Clock Frequency[4]			100	-	400	KHz
Ton Delay/Toff Delay			-	5	-	mS
Ton Delay/Toff Delay Range	Set by PMBus™ command		2	-	5000	mS
Ramp Delay/Toff Delay Accuracy	Turn on,Turn off delay		0	-	+2	mS
Ton Ramp/Toff Ramp Duration	Default (2 phase or 2 channel only)		-	5	10	mS
Power Good V_O Threshold			85	90	95	%
Power Good V_O Hysteresis			-	5	10	%
Power Good Delay Applies to turn-on only (Low to High transition)	Factory Default Set using PMBus™		- 0	1 -	2 5000	mS mS
Power Good Low Voltage	Vin from 0-14V		-	-	0.5	V
CMTBF	Calculated according to Bellcore or Telcordia TR-NTW-000332 at 40C full-load		50	-	-	MHours

Note 1 - Vo measured at the termination of the VSx+ and VSx- sense points across line, load, temperature variation.
Note 2 - Vo1 and Vo2 are the outputs of dual output module.
Note 3 - Dual mode (2 outputs): 2 x 680uF/6.3V Polymer Tan caps (T530X687M006ATE010 or equivalent)
+ 8 x 100uF/6.3V X6S 1210 ceramic caps (GRM32EC80J107ME20L or equivalent)
+ 4x10uF/16V X6S 0603 ceramic caps (GRM188C81C106MA73 or equivalent)
Single mode (1 output): 2 x 680uF/6.3V Polymer Tan caps (T530X687M006ATE010 or equivalent)
+ 10 x 100uF/6.3V X6S 1210 ceramic caps (GRM32EC80J107ME20L or equivalent)
+ 4x10uF/16V X6S 0603 ceramic caps (GRM188C81C106MA73 or equivalent)
Note 4 - For operation PMBus clock frequency at 400kHz, see PMBus™ Power System Management Protocol Specification for timing parameter limits.
Note 5 - For dual outputs condition, the switching frequency of both outputs must be the same. Also, must use the higher switching frequency between the 2 outputs. For example, if Vout1 = 0.6V and Vout2= 3.3V, the switching frequency for both outputs must be set to 800kHz.

Output Specifications

Table 3. Output Specifications, con't:

Parameter	Conditions	Symbol	Min	Nom	Max	Unit
Shelf Life	Calculated at 40 ^{O}C		2	-	-	Years
Over Voltage Protection	All		-	110	-	%V_O
Over Current Protection[6]	Io1,Io2		-	31	36	A
Over Temperature Protection	All		-	110	125	^{O}C

Note 6 - The OCP set point applies per phase. The total OCP current value will be twice of Io1 in single mode.

Performance Curves – 2 Outputs (Efficiency at different Vin)

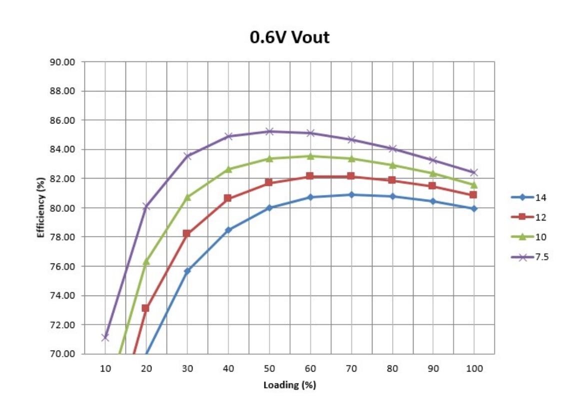


Figure 1: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 25A, Vo= 0.6V, 2output , Frequency=615KHz

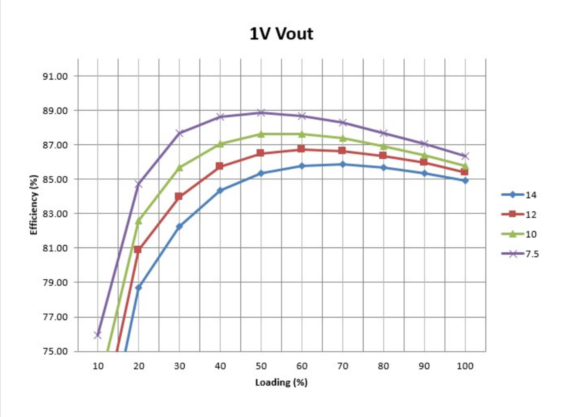


Figure 2: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 25A, Vo= 1V, 2output , Frequency=615KHz

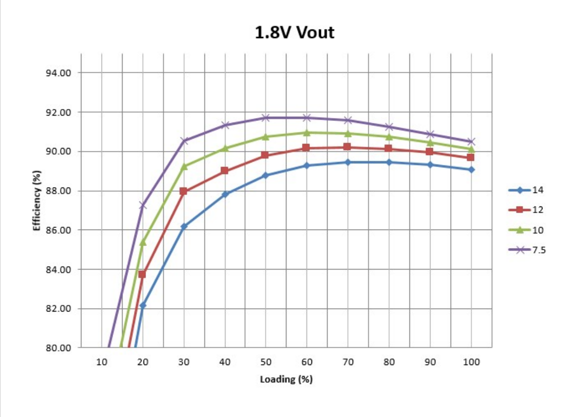


Figure 3: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 22.5A, Vo= 1.8V, 2output , Frequency=800KHz

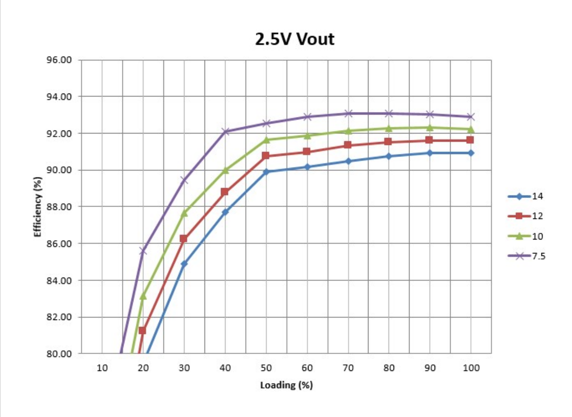


Figure 4: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 17A, Vo= 2.5V, 2output , Frequency=800KHz

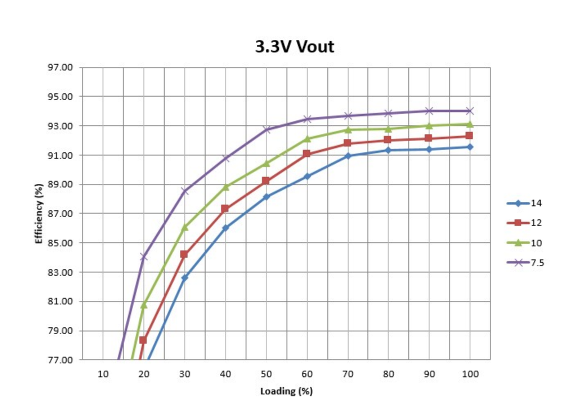


Figure 5: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 14A, Vo= 3.3V, 2 output , Frequency=800KHz

Performance Curves – 2 phases single output (Efficiency at different Vin)

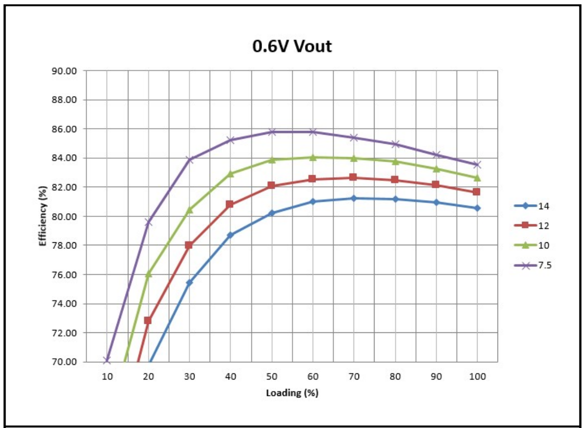


Figure 6: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 50A, Vo= 0.6V, 2 phase, Frequency=615KHz

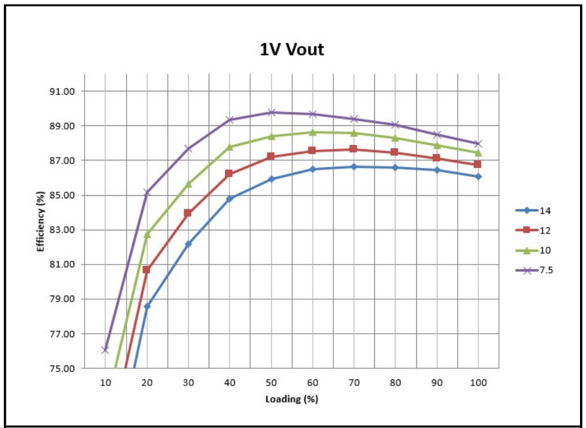


Figure 7: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 50A, Vo= 1V , 2 phase, Frequency=615KHz

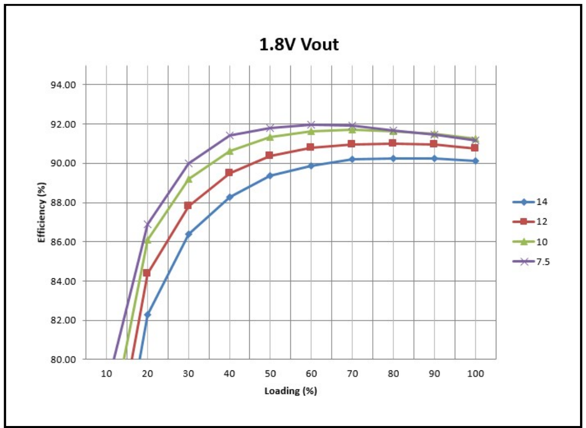


Figure 8: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 45A, Vo= 1.8V ,2 phase, Frequency=800KHz

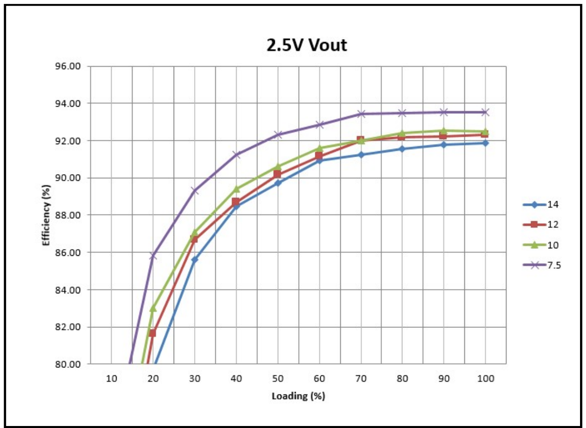


Figure 9: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 34A, Vo= 2.5V , 2 phase, Frequency=800KHz

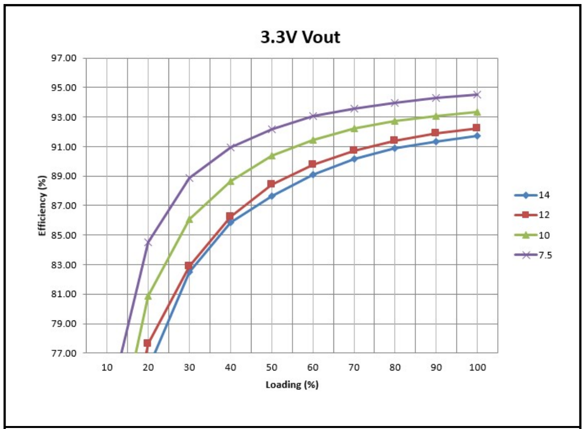


Figure 10: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 28A, Vo= 3.3V, 2 phase , Frequency=800KHz

Performance Curves – 2 Outputs (Efficiency at different switching frequency)

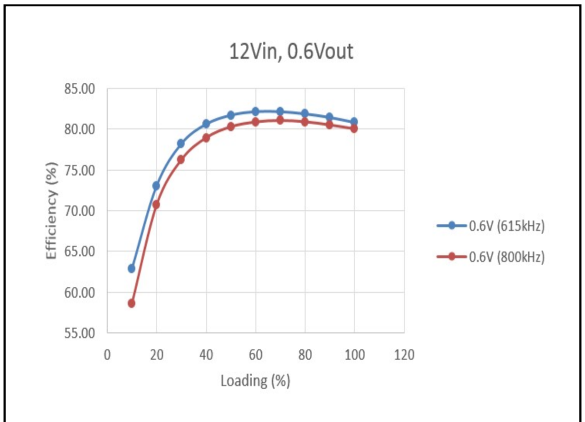


Figure 11: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 25A , Vo= 0.6V , 2 output

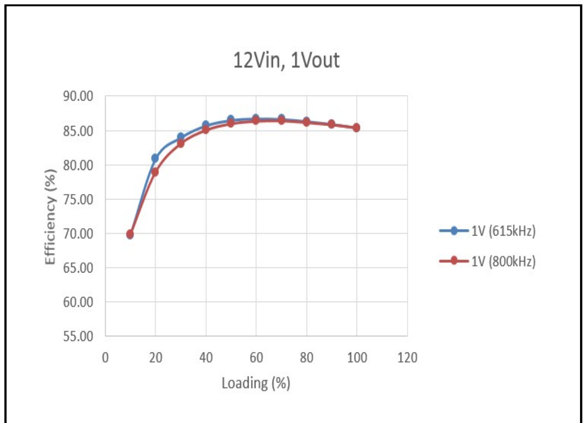


Figure 12: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 25A , Vo= 1V , 2 output

Performance Curves – 2 Phases Single Output (Efficiency at different switching frequency)

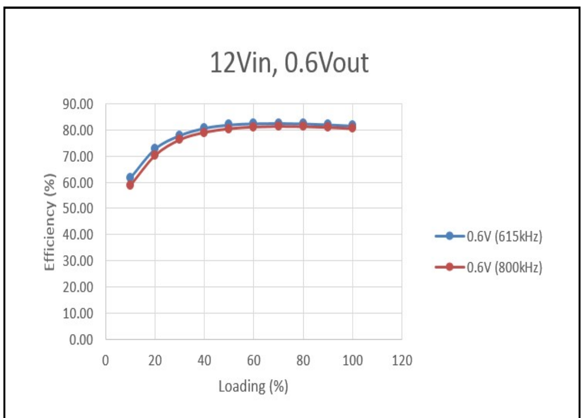


Figure 13: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 50A , Vo= 0.6V , 2Phase

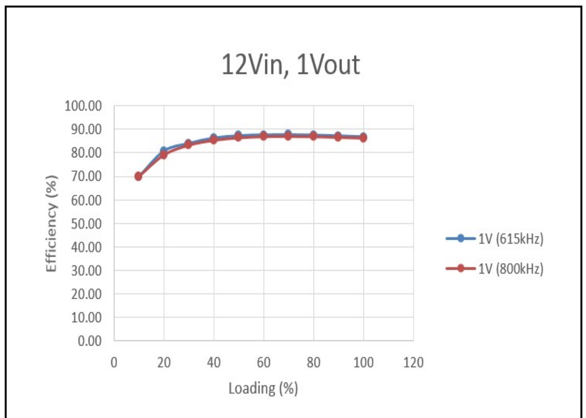


Figure 14: Efficiency Curves @ 25 degC

Loading: Io = 10% increment to 50A , Vo= 1V , 2Phase

Performance Curves – 2 modules (Airflow Thermal derating)

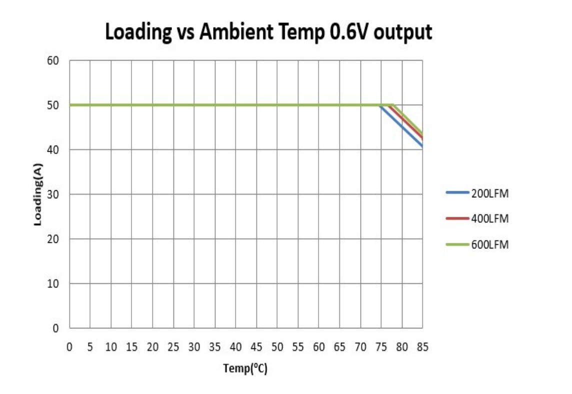


Figure 15: Airflow Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 14V Load: Io= 0 to 50A, Vo= 0.6V Fsw=615kHz

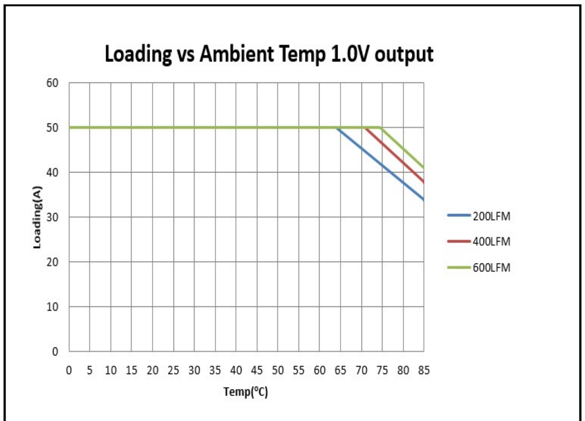


Figure 16: Airflow Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 14V Load: Io= 0 to 50A, Vo= 1V Fsw=615kHz

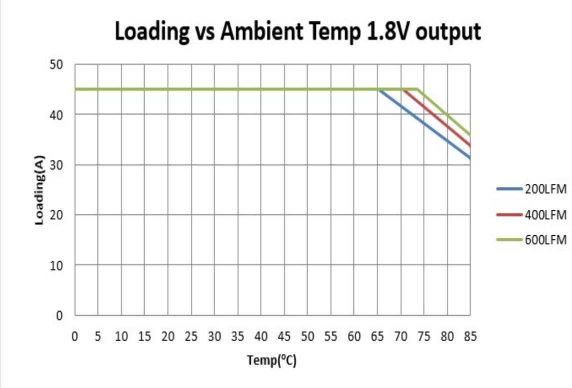


Figure 17: Airflow Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 45A, Vo=1.8V Fsw=800kHz

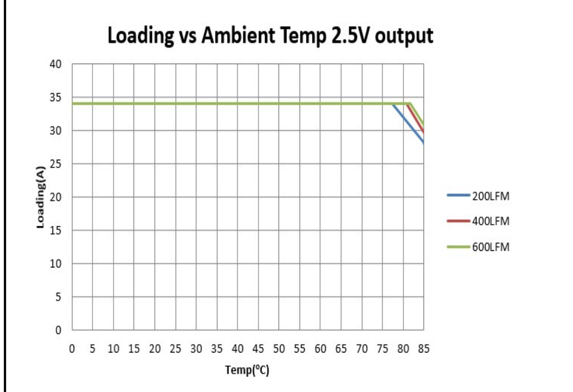


Figure 18: Airflow Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 34A, Vo=2.5V Fsw=800kHz

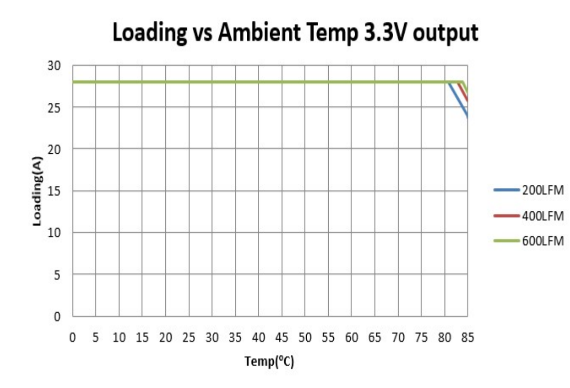


Figure 19: Airflow Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 28A, Vo=3.3V Fsw=800kHz

Note: The thermal performance of one module is much better than two modules.

Performance Curves – 2 modules (E-Cooling Thermal derating)

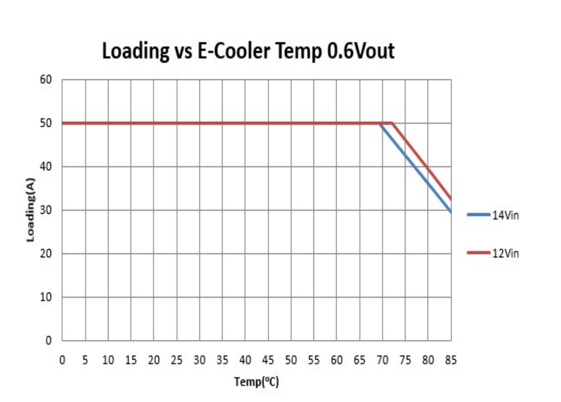


Figure 20: E-Cooling Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 14V Load: Io= 0 to 50A, Vo= 0.6V Fsw=615kHz

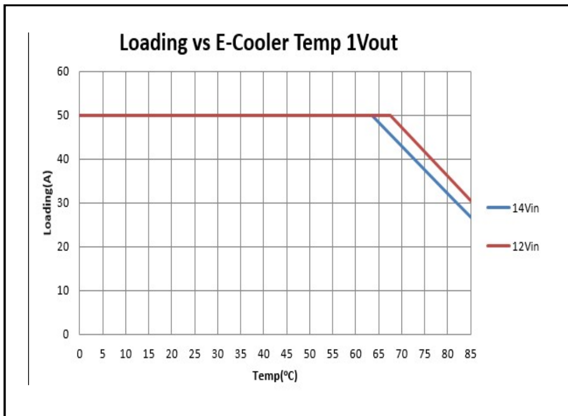


Figure 21: E-Cooling Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 14V Load: Io= 0 to 50A, Vo= 1V Fsw=615kHz

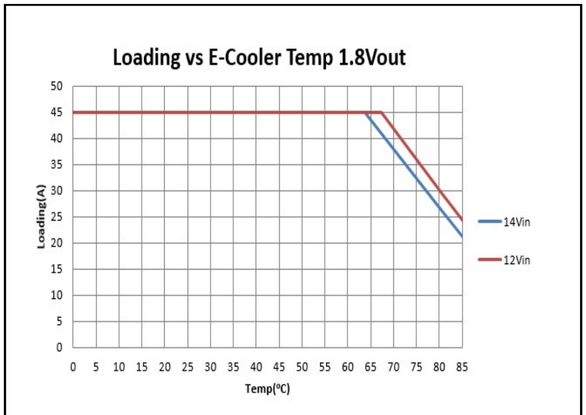


Figure 22: E-Cooling Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 45A, Vo=1.8V Fsw=800kHz

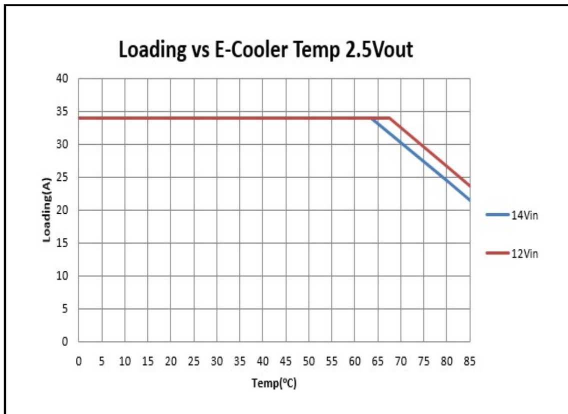


Figure 23: E-Cooling Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 34A, Vo=2.5V Fsw=800kHz

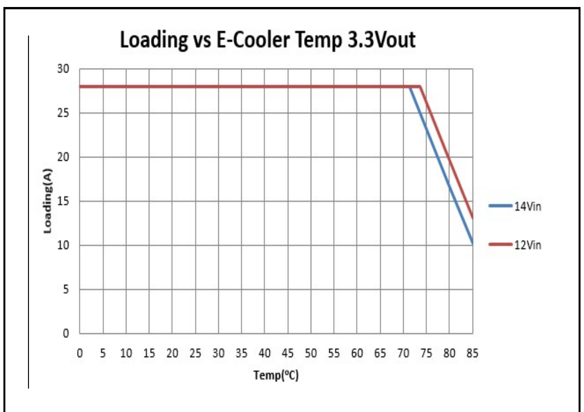


Figure 24: E-Cooling Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 28A, Vo=3.3V Fsw=800kHz

Note: The thermal performance of one module is much better than two modules.
E-Cooling Thermal Derating test setup : The E-cooling is applied at the bottom side of a 8 layers' Demo board and the two modules are placed at top side of the 8 layers' demo board.

Performance Curves – 2 modules (Natural Cooling System Thermal derating)

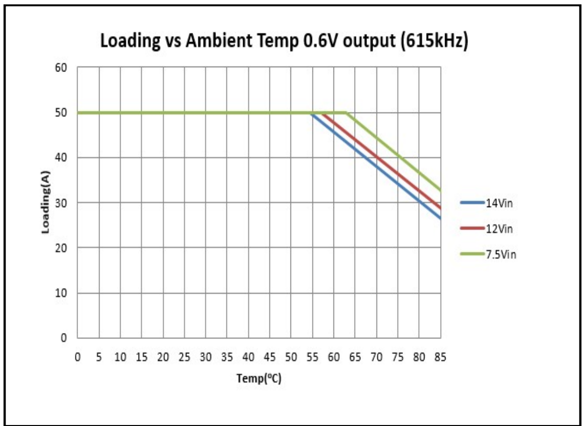


Figure 25: Natural Cooling Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 14V Load: Io= 0 to 50A, Vo= 0.6V Fsw=615kHz

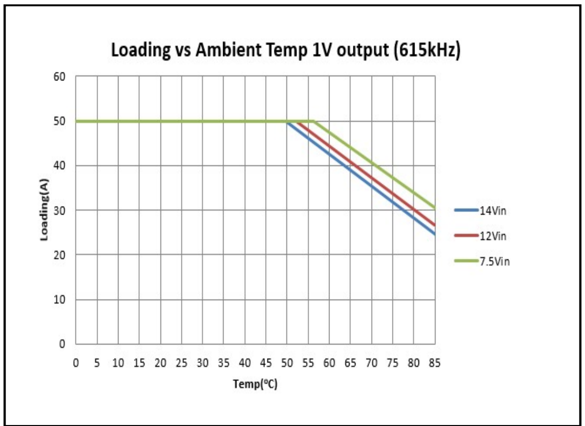


Figure 26: Natural Cooling Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 14V Load: Io= 0 to 50A, Vo= 1V Fsw=615kHz

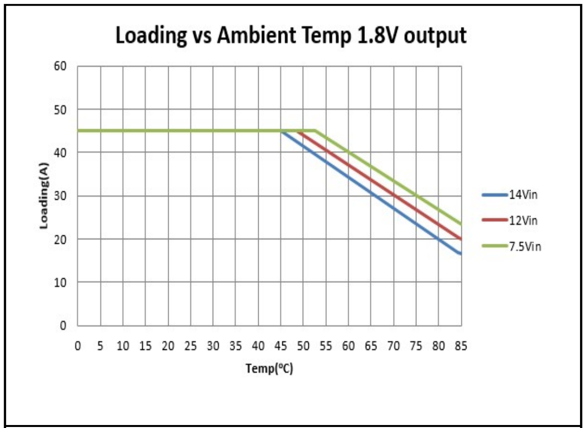


Figure 27: Natural Cooling Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 45A, Vo=1.8V Fsw=800kHz

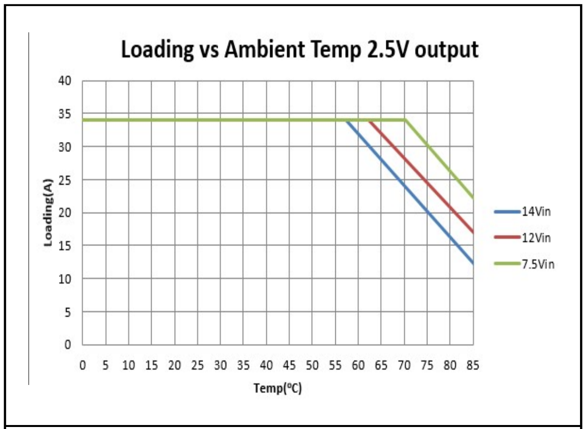


Figure 28: Natural Cooling Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 34A, Vo=2.5V Fsw=800kHz

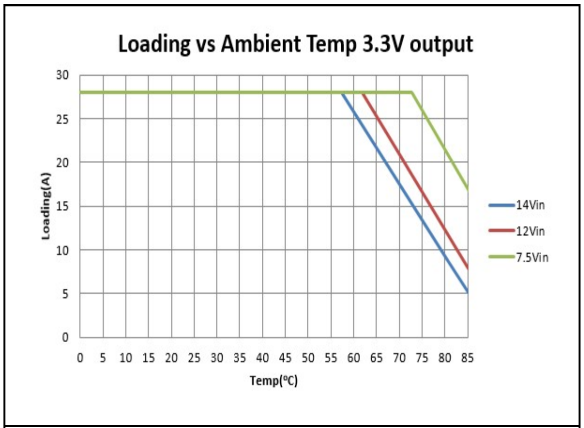


Figure 29: Natural Cooling Thermal Derating Curves (Two modules with Longitudinal airflow)
Vin= 14V Load: Io= 0 to 28A, Vo=3.3V Fsw=800kHz

Note: The thermal performance of one module is much better than two modules.

Performance Curves (Output ripple)

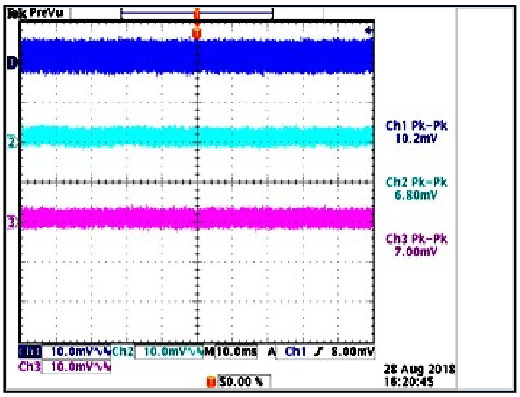


Figure 30: Ripple and Noise - Vo= 0.6V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3

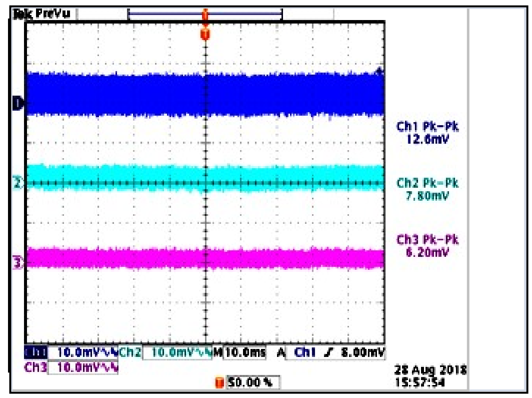


Figure 31: Ripple and Noise - Vo= 1.0V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3

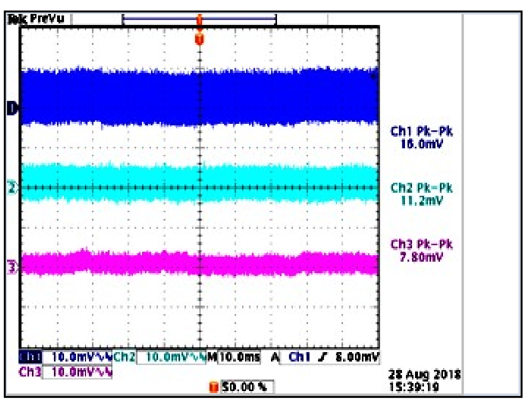


Figure 32: Ripple and Noise - Vo= 1.8V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3

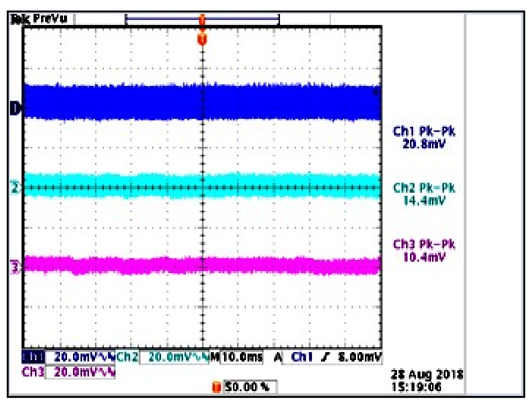


Figure 33: Ripple and Noise - Vo= 2.5V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3

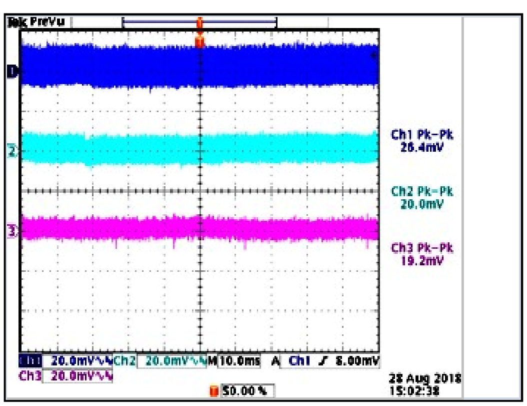


Figure 34: Ripple and Noise - Vo= 3.3V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3

Note: Vo1 and Vo2 are the outputs of dual output module Vo3 is the output of single output module

Performance Curves (Start Up)

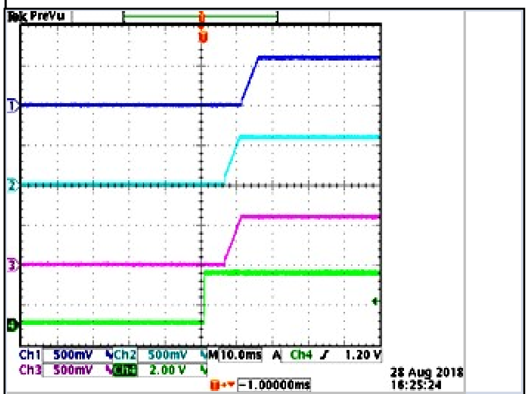


Figure 35: Start Up - Vo= 0.6V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3 Ch4: Enable

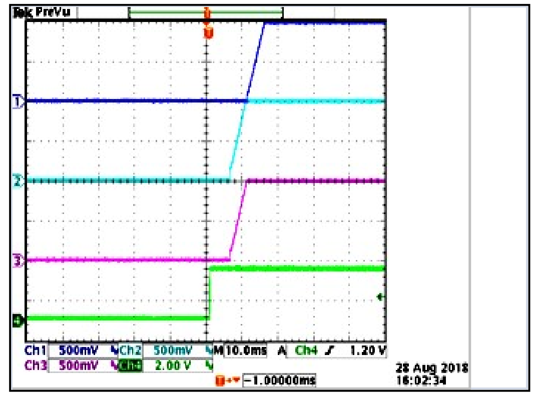


Figure 36: Start Up - Vo= 1V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3 Ch4: Enable

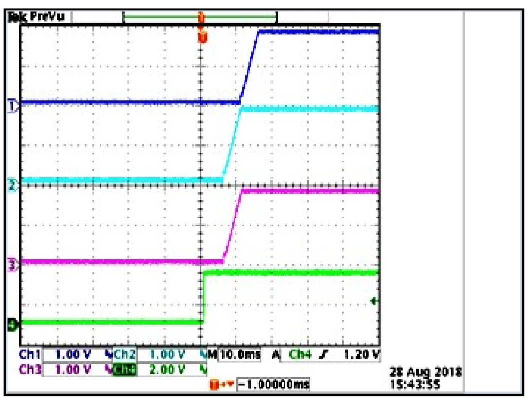


Figure 37: Start Up - Vo= 1.8V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3 Ch4: Enable

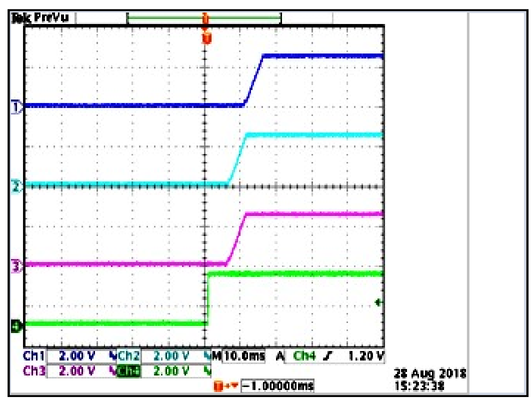


Figure 38: Start Up - Vo= 2.5V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3 Ch4: Enable

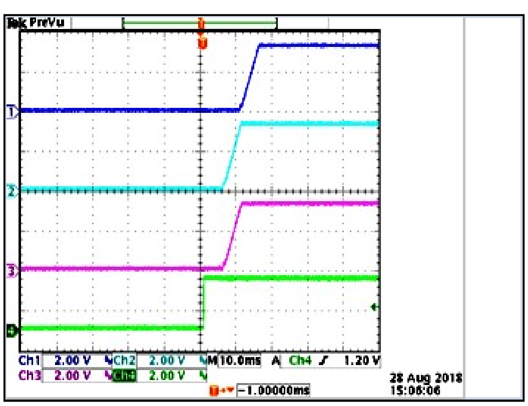


Figure 39: Start Up - Vo= 3.3V
Full Load
Ch 1: Vo1 Ch 2: Vo2 Ch 3: Vo3 Ch4: Enable

Note: Vo1 and Vo2 are the outputs of dual output module Vo3 is the output of single output module

Performance Curves (Slow Dynamic load response – 2phase 2 output)

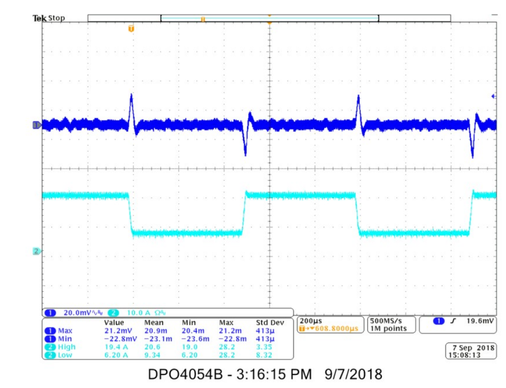


Figure 40: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 0.6V
Ch 1: Io Ch 2 : Vo Fsw=615kHz

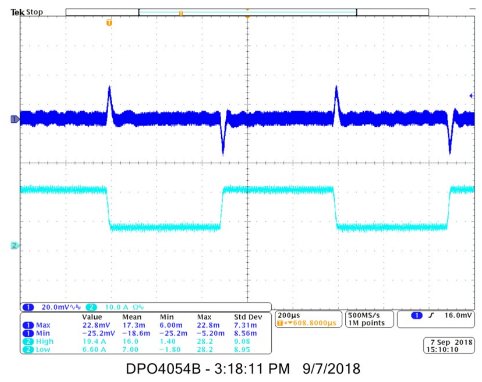


Figure 41: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 1.0V
Ch 1: Io Ch 2 : Vo Fsw=615kHz

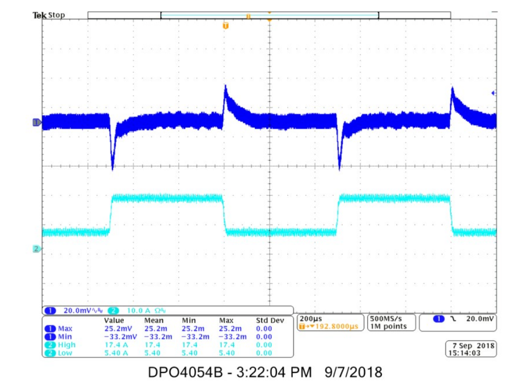


Figure 42: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 1.8V
Ch 1: Io Ch 2 : Vo Fsw=800kHz

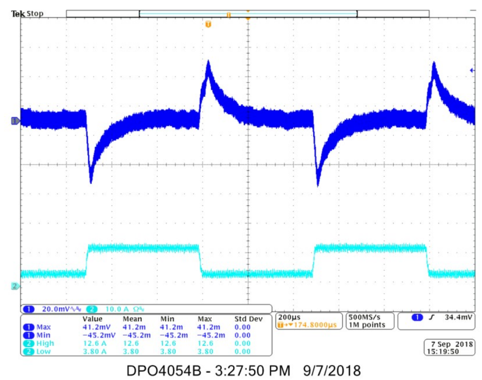


Figure 43: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 2.5V
Ch 1: Io Ch 2 : Vo Fsw=800kHz

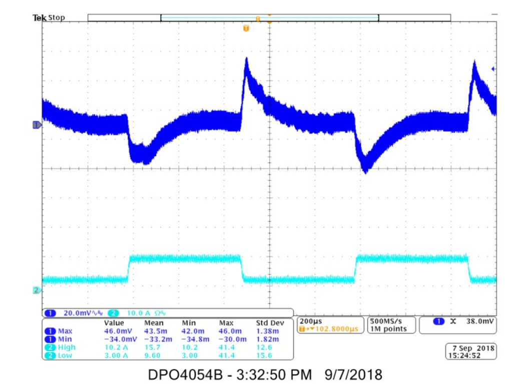


Figure 44: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 3.3V
Ch 1: Io Ch 2 : Vo Fsw=800kHz

Performance Curves (Slow Dynamic load response – 2phase 1 output)

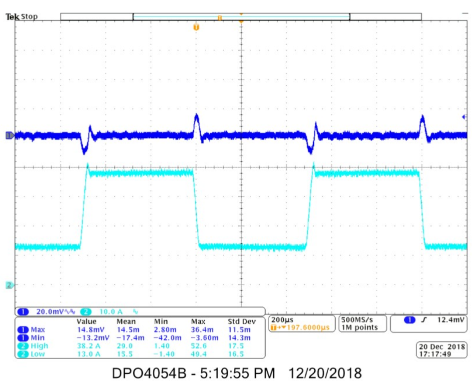


Figure 45: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 0.6V
Ch 1: Io Ch 2 : Vo Fsw=615kHz

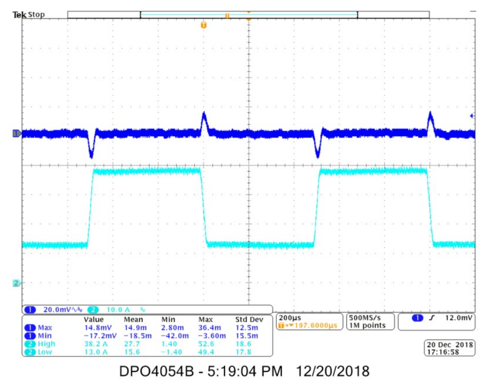


Figure 46: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 1.0V
Ch 1: Io Ch 2 : Vo Fsw=615kHz

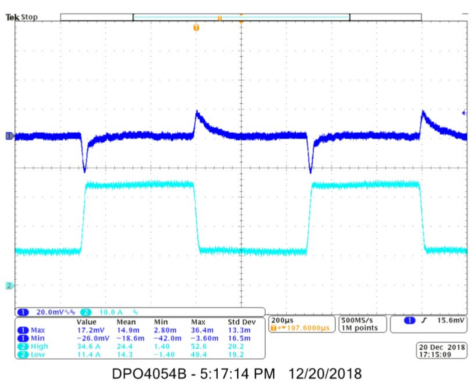


Figure 47: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 1.8V
Ch 1: Io Ch 2 : Vo Fsw=800kHz

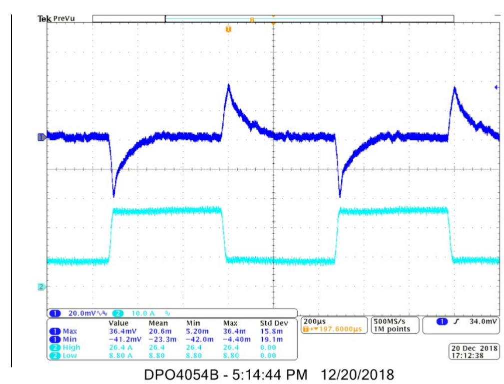


Figure 48: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 2.5V
Ch 1: Io Ch 2 : Vo Fsw=800kHz

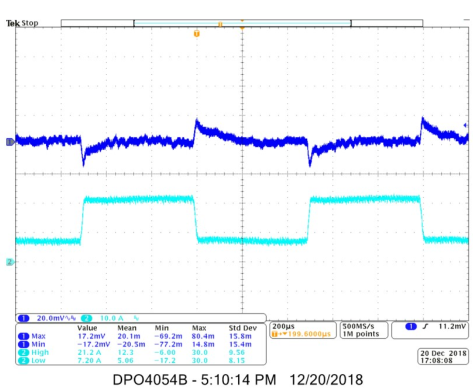


Figure 49: Transient Response – Vo Deviation
25% to 75% to 25% load change, 1A/µS slew rate, Vin = 12Vdc Vo= 3.3V
Ch 1: Io Ch 2 : Vo Fsw=800kHz

Performance Curves (Fast Dynamic load response – 2 Phase 2 Outputs)

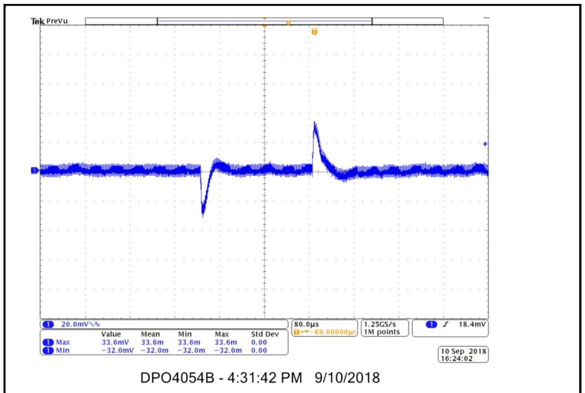


Figure 50: Transient Response – Vo Deviation
25% to 75% to 25% load change, 100A/µS slew rate, Vin = 12Vdc - Vo= 1V
Ch 1: Vo, Fsw=615kHz

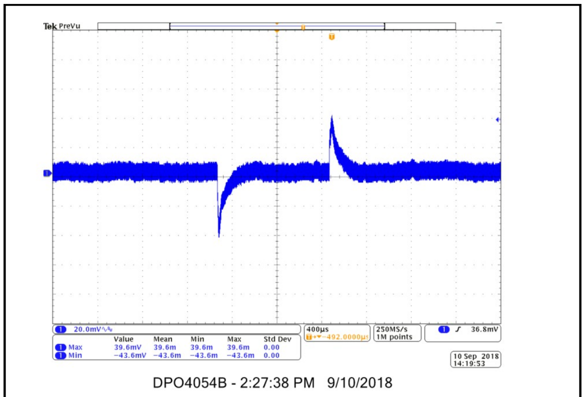


Figure 51: Transient Response – Vo Deviation
25% to 75% to 25% load change, 100A/µS slew rate, Vin = 12Vdc - Vo= 2V5
Ch 1: Vo, Fsw=800kHz

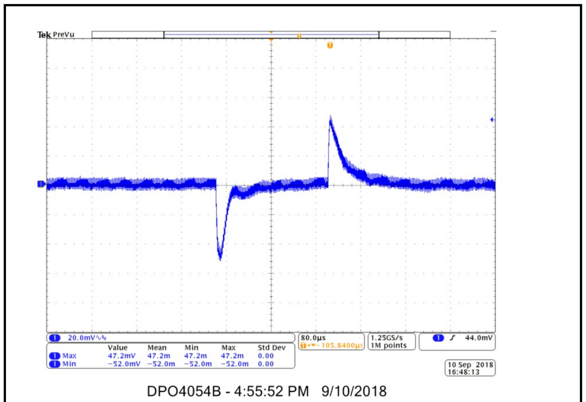


Figure 52: Transient Response – Vo Deviation
10% to 90% to 10% load change, 100A/µS slew rate, Vin = 12Vdc - Vo= 1V
Ch 1: Vo, Fsw=615kHz

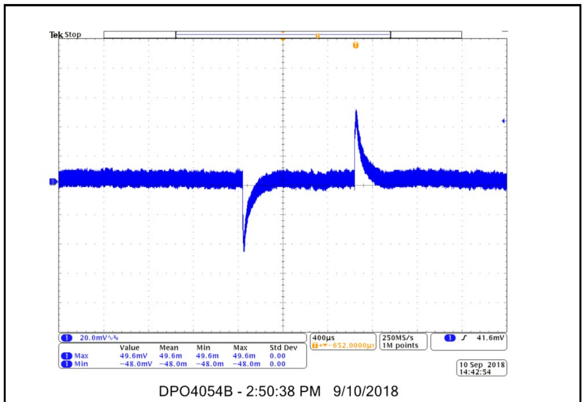


Figure 53: Transient Response – Vo Deviation
10% to 90% to 10% load change, 100A/µS slew rate, Vin = 12Vdc - Vo= 2V5
Ch 1: Vo, Fsw=800kHz

Performance Curves (Fast Dynamic load response – 2 Phase Single Output)

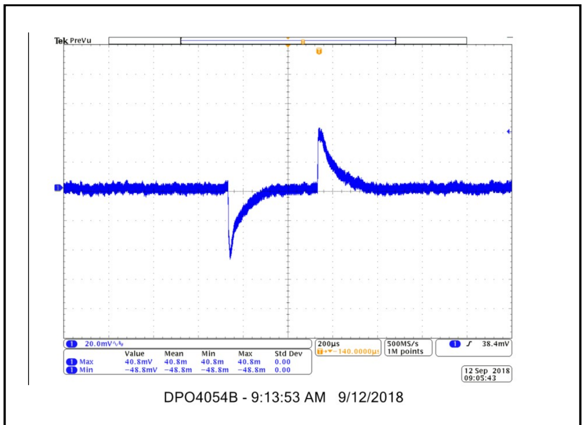


Figure 54: Transient Response – Vo Deviation
25% to 75% to 25% load change, 100A/µS slew rate, Vin = 12Vdc - Vo= 2V5
Ch 1: Vo, Fsw=800kHz

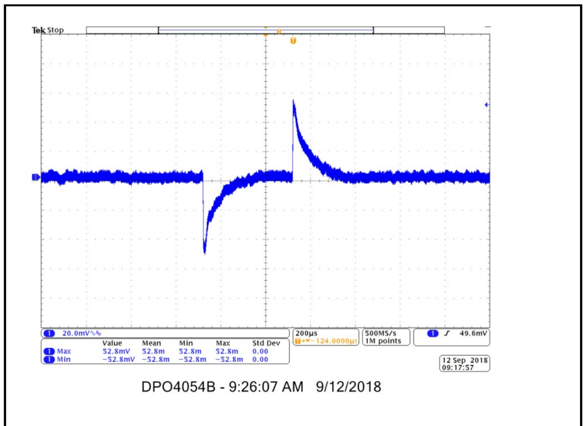


Figure 55: Transient Response – Vo Deviation
10% to 90% to 10% load change, 100A/µS slew rate, Vin = 12Vdc - Vo= 2V5
Ch 1: Vo, Fsw=800kHz

Protection Function Specification

Output Overvoltage Protection

The LGA50D offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VS pin) to a programmable threshold set to 10% higher than the target output voltage (the default setting).

If the VS voltage exceeds this threshold, the PG pin will de-assert and the module will latch.

Output Pre-Bias Protection

The LGA50D provides pre-biased start-up operation in 2 output and single module 2 phase operation. Pre-Bias protection is not provided when operating in current sharing 4, 6 or 8 phase configurations. An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output.

The LGA50D provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the desired output voltage is present after the Ton-delay time the LGA50D starts switching with a duty cycle that matches the pre-bias voltage. This ensures that the ramp-up from the pre-bias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE command.

The resulting output voltage rise time will vary depending on the pre-bias voltage, but the total time elapsed from the end of the Ton-delay time to when the Ton-rise time is complete and the output is at the desired value will match the pre-configured ramp time. See Figure 56 and Figure 57.

If a pre-bias voltage higher than the target voltage exists after the pre-configured Ton-delay time and Ton-rise time have completed, the LGA50D starts switching with a duty cycle that matches the pre-bias voltage. This ensures that the ramp-down from the pre-bias voltage is monotonic. The output voltage is then ramped down to the desired output voltage

If a pre-bias voltage higher than the overvoltage limit exists, the module will not initiate a turn-on sequence and will stay off with an output OV fault recorded.

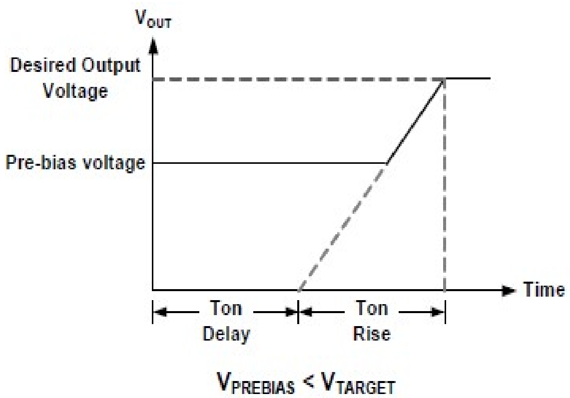


Figure 56

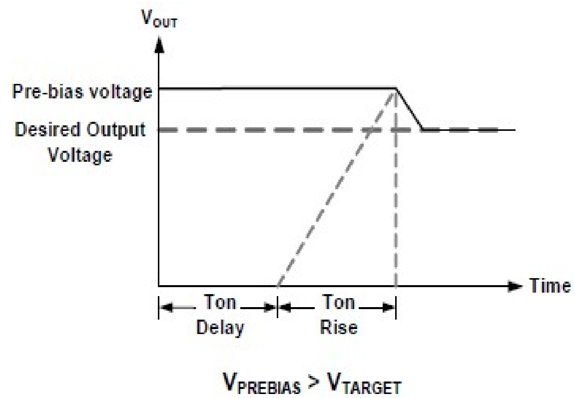


Figure 57

Input Voltage Undervoltage Lock-Out Setting (UVLO)

The input undervoltage lockout (UVLO) prevents the LGA50D from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The input voltage undervoltage lock-out threshold can be set between 4.18V and16V using the VIN_UV_FAULT_LIMIT command. The default UVLO ON and OFF value are 7.2V.and 6.9V respectively.
The default response from an undervoltage fault is to shutdown and stay off until the fault has cleared and the module has been disabled and re-enabled.

When controlling the LGA50D exclusively through the PMBus™, a high voltage setting for UVLO can be used to prevent the LGA50D from being enabled until a lower voltage for UVLO is set using the VIN_UV_FAULT_LIMIT command.

Output Over Current Protection

The LGA50D can protect the power supply from damage from an overloaded or shorted output. Once the current trigger OCP set point, the unit will latch.

Over Temperature Protection

The LGA50D provide over temperature protection where the hotspot of the module. There are two over temperature protection sensing point, one is on the controller IC, the other one is on the Mosfet.

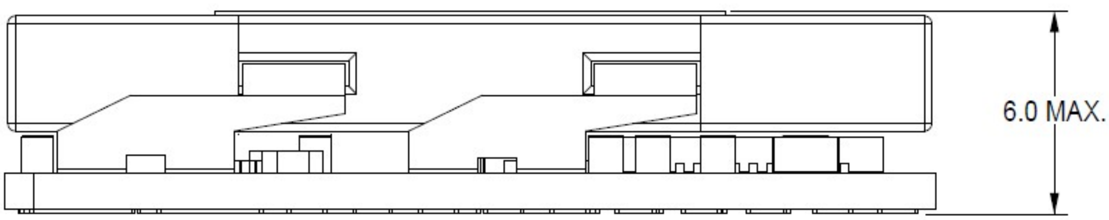
Once the module has been disabled due to over temperature fault, the unit will auto recovery once temperature is below typical 110°C of OT_WARN_LIMIT

Mechanical Specifications

Mechanical Drawing (Dimensioning and Mounting Locations)

Side view of standard solder bump termination type (LGA50D-01DADJLPJ/LGA50D-01DADJLP1J)

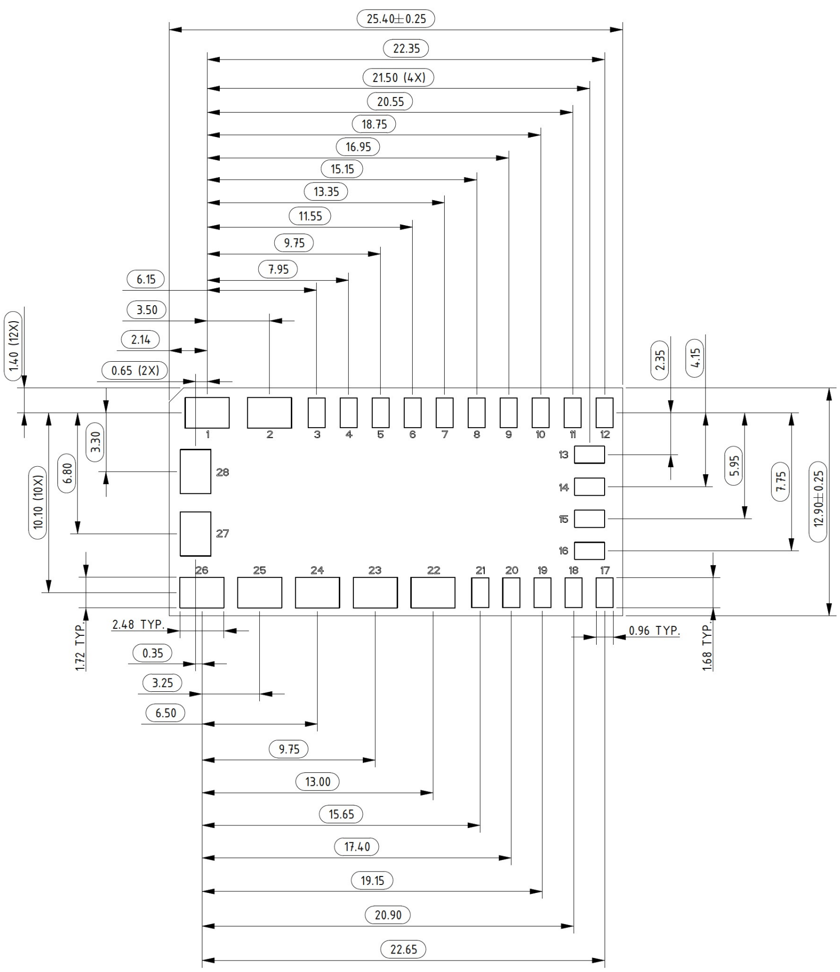
Maximum Weight = 7.3 g



Mechanical Drawing (Dimensioning and Mounting Locations)

Footprint Drawing of Solder Bumps (Bottom View)

For standard solder bump pin termination ((LGA50D-01DADJLPJ/LGA50D-01DADJLP1J)



Recommended Pad Layout

Table 4. Pin Assignments:

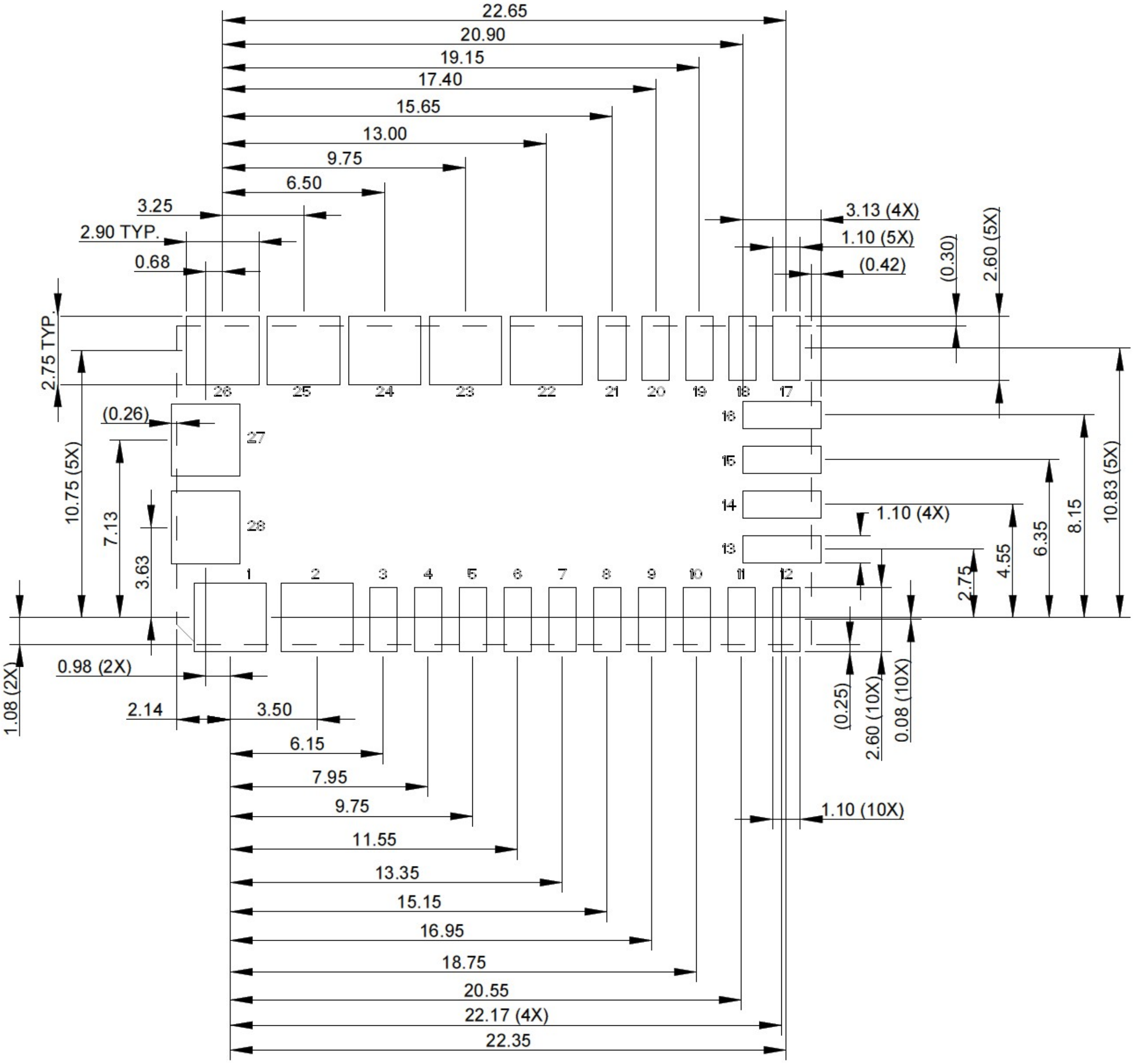
Pin #	Function	Pin #	Function
1	Vin	15	CFG
2	GND	16	Vtrim1
3	PG1	17	VS1+
4	PG2	18	VS1-
5	EN1	19	Vtrim2
6	EN2	20	VS2-
7	SYNC	21	VS2+
8	SHARE	22	Vo1
9	ADDR	23	Vo1
10	SCL	24	GND
11	SDA	25	Vo2
12	SALERT	26	Vo2
13	SGND	27	GND
14	ASCRCFG	28	Vin

Notes: REMARKS: Dimensions are in millimeters
Tolerance: X.XXmm±0.25mm

Mechanical Drawing (Dimensioning and Mounting Locations)

Proposed solder pad macros for standard solder bump termination

(LGA50D-01DADJLPJ/LGA50D-01DADJLP1J).



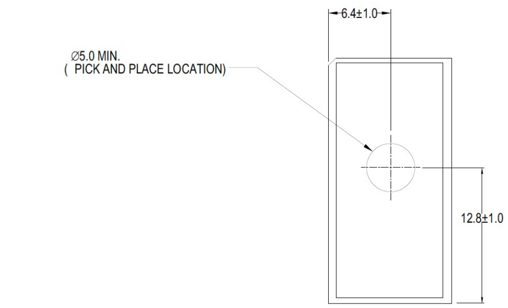
Recommended Pad Layout

REMARKS: Dimensions are in millimeters
Tolerance: X.XXmm±0.25mm
DOT LINE REPRESENTS LGA50D MODULE OUTLINE

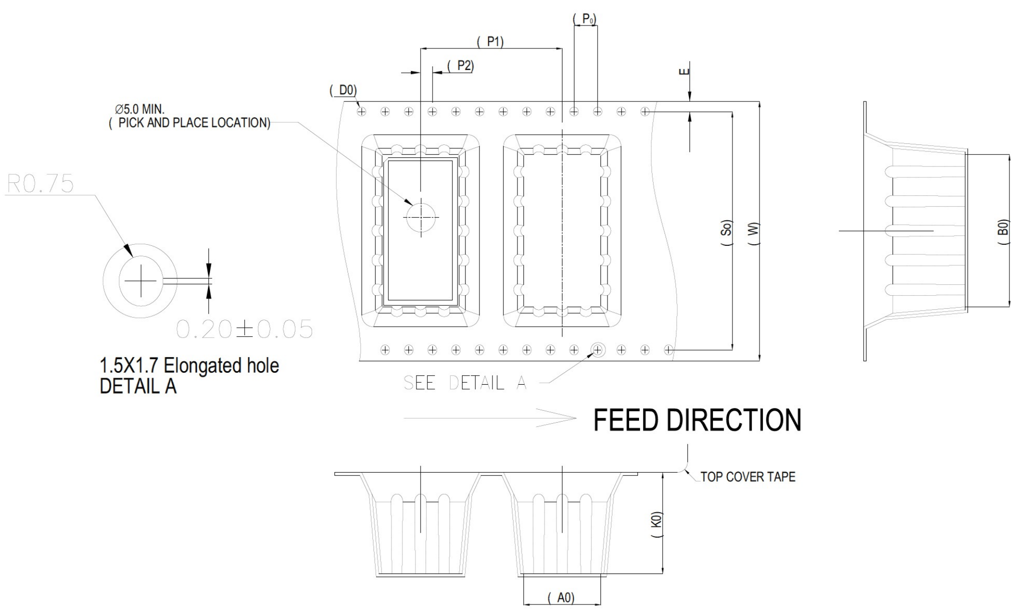
Mechanical Considerations

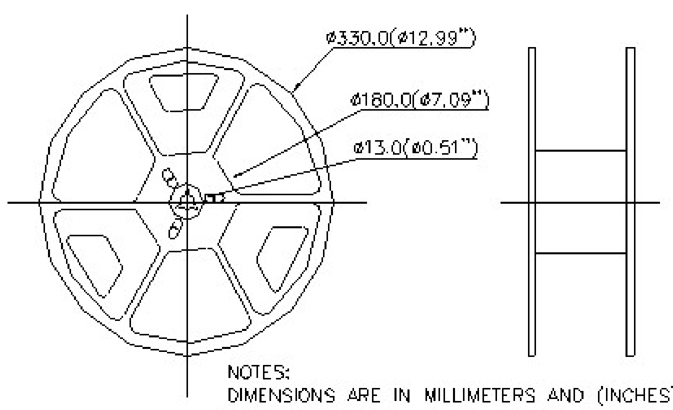
Surface Mount Tape & Reel

LGA50D-01DADJLPJ/LGA50D-01DADJLP1J



EIA DIMENSIONS	
W	44.00±0.30
E	1.75±0.10
P_1	20.00±0.10
P_0	4.00±0.10
P_2	2.00±0.15
D_0	⌀1.50 $^{+0.10}_{-0.00}$
S_0	40.40±0.10
A_0	13.10±0.10
B_0	25.70±0.10
K_0	6.10±0.10





NOTES:
DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCES: X.Xmm±0.5mm(X.XX in.±0.02 in.)
X.XXmm±0.25mm(X.XXX in.±0.010 in.)

Power and Control Signal Descriptions

Table 5. Power and Control Signal Descriptions:

PIN#	Name	Type[1]	Function
1	Vin	PWR	Input positive power pin.
2	GND	PWR	Power ground pin.
3	PG1	O	Vo1 power-good output. Default is push-pull, cannot be shorted to PG2.
4	PG2	O	Vo2 power-good output. Default is push-pull, cannot be shorted to PG1.
5	EN1	I	Enable Vo1. Active signal enables LGA50D.
6	EN2	I	Enable Vo2. Active signal enables LGA50D.
7	SYNC	M/I/O	Clock synchronization input. Used to set the switching frequency. Refer to Switching Frequency Setting.
8	SHARE	I/O	Single-wire DDC bus (current sharing, LGA50Ds communication).
9	ADDR	M	Serial address select pin. Used to assign unique address for each individual device. Connect resistor to SGND. Refer to Address Setting.
10	SCL	I/O	Serial clock. Connect to external host and/or to other LGA50D.Requires a pull-up resistor to a 2.5V to 5.5V source, the source must be always on.
11	SDA	I/O	Serial data. Connect to external host and/or to other LGA50D.Requires a pull-up resistor to a 2.5V to 5.5V source, the source must be always on.
12	ALERT	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 2.5V to 5.5V source, the source must be always on.
13	SGND	PWR	Signal ground. SGND is shorted to GND internally on LGA50D.
14	ASCRCFG	M	Control loop configuration settings. Refer to control Loop(ASCR) Setting.
15	CFG	M	Setting operating mode. Refer to Configuration Setting.
16	Vtrim1	M	Setting output voltage Vo1. Connect resistor to SGND. Refer to Output Voltage Setting.
17	VS1+	I	Differential output Vo1 voltage sense feedback. Connect to positive output regulation point.
18	VS1-	I	Differential output Vo1 voltage sense feedback. Connect to negative output regulation point.
19	Vtrim2	M	Setting output voltage Vo2. Connect resistor to SGND. Refer to Output Voltage Setting.
20	VS2-	I	Differential output Vo2 voltage sense feedback. Connect to negative output regulation point.
21	VS2+	I	Differential output Vo2 voltage sense feedback. Connect to positive output regulation point.

Power and Control Signal Descriptions Con't

Table 5. Power and Control Signal Descriptions Con't:

PIN#	Name	Type	Function
22	Vo1	PWR	Output Vo1 positive power pin.
23	Vo1	PWR	Output Vo1 positive power pin.
24	GND	PWR	Power ground pin.
25	Vo2	PWR	Output Vo2 positive power pin.
26	Vo2	PWR	Output Vo2 positive power pin.
27	GND	PWR	Power ground pin.
28	Vin	PWR	Input positive power pin.

Note 1 - I = Input, O = Output, PWR = Power or Ground, M = Multimode pins.

PMBus™ Interface Support

PMBus™ Communications

The LGA50D provides a SMBus digital interface. The LGA50D can be used with any standard 2-wire SMBus host module. In addition, the module is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during module power-up. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any module to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the module monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the LGA50D (nominally 4mA). A pull-up resistor of 10kΩ is a good value for most applications.

SMBus Data and Clock lines should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0V and 0.8V respectively will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 10 modules on an SMBus a 10kΩ resistor on each line provides good performance.

The LGA50D accepts most standard PMBus™ commands. When enabling the module with ON_OFF_CONFIG command, it is recommended that the enable pin is tied to SGND.

In addition to bus noise considerations, it is important to ensure that user connections to the SMBus are compliant to the PMBus™ command standards. Any module that can malfunction in a way that permanently shorts SMBus lines will disable PMBus™ communications. Incomplete PMBus™ commands can also cause the LGA50D to halt PMBus™ communications. This can be corrected by disabling, then re-enabling the module.

Monitoring via PMBus™

A system controller can monitor a wide variety of different LGA50D parameters through the SMBus interface. The module can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of pre-configured fault conditions occur.

The module can also be monitored continuously for any number of power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Fault status information

The PMBus™ Host should respond to SALRT as follows:

1. LGA50D module pulls SALRT Low.
2. PMBus™ Host detects that SALRT is now low, performs transmission with Alert Response Address to find which LGA50D module is pulling SALRT low
3. PMBus™ Host talks to the LGA50D module that has pulled SALRT low.

The actions that the host performs are up to the System Designer.

If multiple modules are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to the PMBus™ Commands section of this document for details on how to monitor specific parameters via the SMBus interface.

PMBus™ SUMMARY

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
00h	PAGE	00h	R/W	1	BIT	Selects Controller 0, 1, or both Page 0 Controller addressed
01h	OPERATION	00h	R/W	1	BIT	Enable/disable, margin settings. Immediate off, nominal margin.
02h	ON_OFF_CONFIG	17h	R/W	1	BIT	On/off configuration settings ENABLE pin control, active high
03h	CLEAR_FAULTS	N/A	Write	N/A	N/A	Clears faults
15h	STORE_USER_ALL	N/A	Write	N/A	N/A	Stores values to user store
16h	RESTORE_USER_ALL	N/A	Write	N/A	N/A	Restores values from user store
21h	VOUT_COMMAND	N/A	R/W	N/A	L16u	Pin Strap Setting. Sets nominal VOUT set-point
22h	VOUT_TRIM	0000h	R/W	2	L16s	Applies offset voltage to VOUT set-point
23h	VOUT_CAL_OFFSET	0000h	R/W	2	L16s	Applies offset voltage to VOUT set-point
24h	VOUT_MAX	N/A	R/W	N/A	L16u	Sets maximum VOUT set-point 1.15*VOUT pin strap-setting
25h	VOUT_MARGIN_HIGH	N/A	R/W	N/A	L16u	Sets VOUT set-point during margin high. 1.05*VOUT pin strap -setting
26h	VOUT_MARGIN_LOW	N/A	R/W	N/A	L16u	Sets VOUT set-point during margin low 0.95*VOUT pin strap- setting
28h	VOUT_DROOP	N/A	R/W	N/A	L11	Sets V/I slope for total rail output current (all phases combined) CFG pin-strap setting
33h	FREQUENCY_SWITCH	N/A	R/W	N/A	L11	Sets switching frequency SYNC pin-strap setting
37h	INTERLEAVE	N/A	R/W	N/A	BIT	Configures phase offset during group Operation Set by pin-strapped PMBus™ address
40h	VOUT_OV_FAULT_LIMIT	N/A	R/W	N/A	L16u	Sets the VOUT overvoltage fault threshold. 1.1xVOUTpinstrapsetting
41h	VOUT_OV_FAULT_RESPONSE	JLPJ = 80h JLP1J = BFh	R/W	1	BIT	Sets the VOUT overvoltage fault response. JLPJ = Disable, no retry JLP1J = Retry continuously, 280ms
44h	VOUT_UV_FAULT_LIMIT	N/A	R/W	N/A	L16u	Sets the VOUT under voltage fault threshold, 0.85xVOUTpinstrapsetting
45h	VOUT_UV_FAULT_RESPONSE	JLPJ = 80h JLP1J = BFh	R/W	1	BIT	Sets the VOUT under voltage fault response JLPJ = Disable, no retry JLP1J = Retry continuously, 280ms
4Fh	OT_FAULT_LIMIT	EBC0B	R/W	2	L11	Sets the over-temperature fault limit. +120° C
50h	OT_FAULT_RESPONSE	FFh	R/W	1	BIT	Sets the over-temperature fault response. Continuous retry, 280ms retry delay
51h	OT_WARN_LIMIT	EB70h	R/W	2	L11	Sets the over-temperature warning limit. +110° C
55h	VIN_OV_FAULT_LIMIT	D3E0h	R/W	2	L11	Sets the VIN overvoltage fault threshold .15.5V
56h	VIN_OV_FAULT_RESPONSE	JLPJ = 80h JLP1J = BFh	R/W	1	BIT	Sets the VIN overvoltage fault response. JLPJ = Disable, no retry JLP1J = Retry continuously, 280ms
57h	VIN_OV_WARN_LIMIT	D3A0h	R/W	2	L11	Sets the VIN overvoltage warning threshold.14.5V
58h	VIN_UV_WARN_LIMIT	CB99	R/W	N/A	L11	Sets the VIN under voltage warning Threshold. 7.195V

PMBus^{TM} SUMMARY

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
59h	VIN_UV_FAULT_LIMIT	CB73	R/W	N/A	L11	Sets the VIN under voltage fault threshold. UVLO pin-strap setting. 6.898V
5Ah	VIN_UV_FAULT_RESPONSE	BFh	R/W	1	BIT	Sets the VIN under voltage fault response. Continuous retries, 280ms retry delay.
5Eh	POWER_GOOD_ON	N/A	R/W	N/A	L16U	Sets the voltage threshold for power-good Indication. 0.9 x VSET pin-strap setting
60h	TON_DELAY	D280h/CA80h	R/W	2	L11	Sets the delay time from enable to VOUT Rise.Vo1=10ms,Vo2=5ms
61h	TON_RISE	CA80h	R/W	2	L11	Sets the rise time of VOUT after ENABLE and TON_DELAY. 5ms
64h	TOFF_DELAY	CA80h	R/W	2	L11	Sets the delay time from DISABLE to start of VOUT fall. 5ms
65h	TOFF_FALL	CA80h	R/W	2	L11	Sets the fall time for VOUT after DISABLE and TOFF_DELAY. 5ms
78h	STATUS_BYTE	00h	R	1	BIT	First byte of STATUS_WORD. No faults
79h	STATUS_WORD	0000h	R	2	BIT	Summary of critical faults. No faults
7Ah	STATUS_VOUT	00h	R	BIT	BIT	Reports VOUT warnings/faults. No faults
7Bh	STATUS_IOUT	00h	R	BIT	BIT	Reports IOUT warnings/faults. No faults
7Ch	STATUS_INPUT	00h	R	BIT	BIT	Reports input warnings/faults. No faults
7Dh	STATUS_TEMP	00h	R	BIT	BIT	Reports temperature warnings/faults. No faults
7Eh	STATUS_CML	00h	R	BIT	BIT	Reports communication, memory, logic Errors. No faults
80h	STATUS_MFR_SPECIFIC	00h	R	BIT	BIT	Reports voltage monitoring/clock synchronization faults. No faults
88h	READ_VIN	N/A	R	N/A	L11	Reports input voltage measurement
8Bh	READ_VOUT	N/A	R	N/A	L16U	Reports output voltage measurement
8Ch	READ_IOUT	N/A	R	N/A	L11	Reports output current measurement
8Dh	READ_TEMPERATURE_1	N/A	R	L11	N/A	Reports internal temperature measurement
8Fh	READ_TEMPERATURE_3	N/A	R	L11	N/A	Reports external temperature measurement from Mosfet pin.
94h	READ_DUTY_CYCLE	N/A	R		L11	Reports actual duty cycle
95h	READ_FREQUENCY	N/A	R		L11	Reports actual switching frequency
98h	PMBus™_REVISION	22h	R	1	BIT	Reports the PMBus™ revision used
99h	MFR_ID	N/A	R/W		ASC	LGA50D-01DADJLPJ/ LGA50D-01DADJLP1J
9Bh	MFR_REVISION	303032	R/W		ASC	Sets a user defined revision.002
9Ch	MFR_LOCATION	N/A	R/W		ASC	Sets a user defined location identifier
9Dh	MFR_DATE	N/A	R/W		ASC	Sets a user defined date
9Eh	MFR_SERIAL	N/A	R/W		ASC	Serial number
B0h	USER_DATA_00	N/A	R/W		ASC	Sets user defined data
D1h	USER_CONFIG	N/A	R/W		BIT	Configures several user-level features Set by CFG pin-strap setting
D3h	DDC_CONFIG	N/A	R/W		BIT	Configures the DDC addressing and current Sharing. Set by pin-strapped PMBus™ address and CFG pin-strap setting
D4h	POWER_GOOD_DELAY	BA00h	R/W	2	L11	Sets the delay between PG threshold and PG assertion
D5h	MULTI_PHASE_RAMP_GAIN	03h	R/W	1	CUS	Adjusts the ramp-up and ramp-down rate by setting the feedback gain

PMBus™ SUMMARY

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
D7h	SNAPSHOT_FAULT_MASK	00h	R/W	1	00h	Masks faults that cause a snapshot to be Taken. No faults masked
DBh	MFR_SMBALERT_MASK	00h	R/W	1	Custom	Identifies which fault limits will not assert SALRT
DDh	PINSTRAP_READ_STATUS	N/A	Read		BIT	Set by pin-straps
DFh	ASCR_CONFIG	N/A	R/W		BIT	Configures the ASCR settings ASCRCFG pin-strap setting
E0h	SEQUENCE	00h	R/W		BIT	DDC rail sequencing configuration Prequel and sequel disabled
E2h	DDC_GROUP	N/A	R/W		BIT	Configures group ID, fault spreading, OPERATION and VOUT Set by CFG pin-strap
E5h	MFR_IOUT_OC_FAULT_RESPONSE	JLPJ = 80h JLP1J = BFh	R/W	1	BIT	Configures the IOUT over current fault Response JLPJ = Disable, no retry JLP1J = Retry continuously, 280ms
E6h	MFR_IOUT_UC_FAULT_RESPONSE	JLPJ = 80h JLP1J = BFh	R/W	1	BIT	Configures the IOUT undercurrent fault Response JLPJ = Disable, no retry JLP1J = Retry continuously, 280ms
E7h	IOUT_AVG_OC_FAULT_LIMIT	DB60h	R/W	L11	L11	Sets the IOUT average over current fault Threshold. 27A
E9h	USER_GLOBAL_CONFIG	N/A	R/W		BIT	Sets options pertaining to advanced Feature. set by CFG pin-strap setting
EAh	SNAPSHOT	N/A	Read		BIT	32-byte read-back of parametric and status values
F0h	LEGACY_FAULT_GROUP	00000000h	R/W		BIT	Configures fault group compatibility with older Intersil digital power devices
F3h	SNAPSHOT_CONTROL	00h	R/W	1	BIT	Snapshot feature control command
F4h	RESTORE_FACTORY	N/A	Write	N/A	N/A	Restores device to the hard-coded default values
F5h	MFR_VMON_OV_FAULT_LIMIT	C266h	R/W	2	L11	Sets the VMON overvoltage fault threshold 2.4V, SPS OT trip voltage
F6h	MFR_VMON_UV_FAULT_LIMIT	9B33h	R/W	2	L11	Sets the VMON under voltage fault Threshold.0.1V, corresponds to -50° C
F7h	MFR_READ_VMON	N/A	Read		L11	Reads the VMON voltage
F8h	VMON_OV_FAULT_RESPONSE	BFh	R/W	1	BIT	Configures the VMON overvoltage fault Response Continuous retry
F9h	VMON_UV_FAULT_RESPONSE	BFh	R/W	1	BIT	Configures the VMON under voltage fault Response. Continuous retry
FAh	SECURITY_LEVEL	01H	Read	1	Hex	Reports the security level Public security level
FBh	PRIVATE_PASSWORD	00…00h	R/W		ASC	Sets the private password string
FCh	PUBLIC_PASSWORD	00…00h	R/W		ASC	Sets the public password string

PMBus™ Use Guidelines

The PMBus™ is a powerful tool that allows the user to optimize circuit performance by configuring the LGA50D for their application. When configuring the LGA50D, the LGA50D should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW and ASCCR_CONFIG. While the LGA50D is enabled any command can be read. Many commands do not take effect until after the LGA50D has been re-enabled, hence the recommendation that commands that change device settings are written while the LGA50D is disabled. When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands. In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

SUMMARY

All commands can be read at any time.

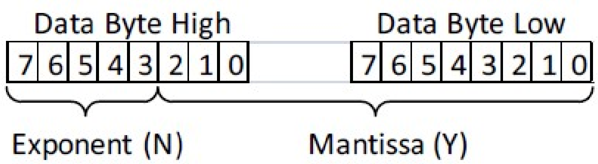
Always disable the LGA50D when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the LGA50D is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to LGA50D setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable the LGA50D.

PMBus™ Data Formats

Linear-11 (L11)

L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal. value (X).



Relation between real world decimal value (X), N and Y $X = Y \cdot 2^N$

Linear-16 Unsigned (L16u)

L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13.}$

Linear-16 Signed (L16s)

L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)

Breakdown of Bit Field is provided in "PMBus™ Command Detail" starting on page 35.

Custom (CUS)

Breakdown of Custom data format is provided in "PMBus™ Command Detail". A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)

A variable length string of text characters uses ASCII data format.

Block R/W type

If command type is Block R/W, please add one bit at the beginning defined data length in bytes.

PMBus™ Command Detail

PAGE (00h)

Definition: Selects phase1(page 01), phase2(page 00) or both phase1 and 2 to receive commands. All commands following this command will be received and acted on by the selected controller or controllers.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: No

Default Value: 00h (Page 0)

Units: N/A

COMMAND	PAGE (00h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:4	BITS 3:0	PAGE
0000	0000	0
0000	0000	1
1111	1111	Both

OPERATION (01h)

Definition: Sets Enable, Disable and VOUT Margin settings. This command can also be monitored to read the operating state of the device on bits 7:6. Writing Immediate off will turn off the output and ignore TOFF_DELAY and TOFF_FALL settings. This command is not stored like other PMBus^{TM} commands. The value read reflects the current state of the device. When this command is written the command takes effect, but if a STORE _USER_ALL written and the device is reenabled, the OPERATION settings may not be the same settings that were written before the device was reenabled.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (immediate off))

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:4	BITS 5:4	BITS 3:0 (NOT USED)	UNIT ON OR OFF	MARGIN STATE
00	00	0000	Immediate off (No sequencing)	N/A
01	00	0000	Soft off (With sequencing)	N/A
10	00	0000	On	Nominal
10	01	0000	On	Margin Low
10	10	0000	On	Margin High

Note: Bit combinations not listed above may cause command errors.

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN). When bit 0 is set to 1(turn off the output immediately), the TOFF_FALL setting is ignored.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 17h (ENABLE pin control, active high, turn off output immediately – no ramp down)

Units: N/A

COMMAND	**ON_OFF_CONFIG (02h)**							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

BIT NUMBER	**PURPOSE**	**BIT VALUE**	**MEANING**
7:5	Not Used	000	Not used
4:2	Sets the default to either operate any time power is present or for the on/off to be controlled by ENABLE pin or OPERATION command	000	Not used
		101	Device starts from ENABLE pin only.
		110	Device starts from OPERATION command only.
1	(Polarity of ENABLE pin - not used)	1	Active high only.
0	ENABLE pin action when commanding the unit to turn off	0	Use the configured ramp-down settings (“soft-off”)
		1	Turn off the output immediately.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Paged or Global: Global

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus™ settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation, the device will be unresponsive for 100ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus™ settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command should not be used during device operation, the device will be unresponsive for 100ms while restoring values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

VOUT_COMMAND (21h)

Definition: This command sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set to be higher than 115% of the pin-strap VSET setting, or VOUT_MAX if VOUT_MAX is set higher than 115% of the pin-strap VSET setting.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: VSET pin-strap setting

Units: Volts

Equation: VOUT = VOUT_COMMAND $\times 2^{-13}$

Range: 0 to VOUT_MAX

Example: VOUT_COMMAND = 699Ah = 27,034

Target voltage equals 27034 $\times 2^{-13}$ = 3.3V

COMMAND	VOUT_COMMAND (21h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	VSET Pin-strap Setting															

VOUT_TRIM (22h)

Definition: The VOUT_TRIM command is used to apply a fixed trim voltage to the output voltage command value. This command is typically used by the manufacturer of a power supply subassembly to calibrate a device in the subassembly circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: Volts

Equation: VOUT trim = VOUT_TRIM×2-13

Range: ±150mV

COMMAND	VOUT_TRIM (22h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_CAL_OFFSET (23h)

Definition: The VOUT_CAL_OFFSET command is used to apply a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: Volts

Equation: VOUT calibration offset = VOUT_CAL_OFFSET×2-13

Range: ±150mVV

COMMAND	**ON_OFF_CONFIG (23h)**															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (24h)

Definition: The VOUT_ MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. If a VOUT_COMMAND is sent with a value higher than VOUT_MAX, the device will set the output voltage to VOUT_MAX. Note that this command setting does not automatically scale with a stored VOUT_COMMAND setting.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.15 x VSET pin-strap setting

Units: Volts

Equation: V_{OUT} max = VOUT_MAX $\times$ 2^{-13}

Range: 0V to 5.5V

COMMAND	VOUT_MAX (24h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.15 x VSET Pin-strap Setting															

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the VOUT during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W word

Protectable: Yes

Default Value: 1.05 x VSET pin-strap setting.

Units: Volts

Equation: VOUT calibration offset = VOUT_CAL_OFFSET $\times$ 2^{-13}

Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_HIGH (25h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VSET Pin-strap Setting															

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the VOUT during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.95 x VSET pin-strap setting

Units: Volts

Equation: VOUT margin low = VOUT_MARGIN_LOW

Range 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_LOW (26h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET Pin-strap Setting															

VOUT_DROOP (28h)

Definition: The VOUT_DROOP sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A at which the output voltage decreases with increasing output current for use with passive current sharing schemes. For devices that are set to sink output current (negative output current), the output voltage continues to increase as the output current is negative. VOUT_DROOP is not needed with a single (2-phase) LGA50D. VOUT_DROOP is needed when multiple LGA50Ds are operated in current sharing mode, i.e., 4-, 6- and 8-phase configurations. In this case, VOUT_DROOP is calculated based on the combined output current of all phases as applicable.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: mV/A

Equation: VOUT_DROOP = $Y \times 2^N$

Range: 0 to 40mV/A

COMMAND	VOUT_DROOP (28h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	Set by CFG Pin-strap Setting															

(TBD) For 4/6/8 phase load regulation, VOUT_DROOP is needed to be considered. The following table is the 4/6/8 phase load regulation requirement.

Parameter	Conditions	Min	Nom	Max	Unit
4/6/8 phase Load Regulation	0.6V ≤ Vo ≤ 1.0V 1.0V < Vo ≤ 5.0V	- -	I_O x VOUT_DROOP + 5 I_O x VOUT_DROOP + V_O x 5	I_O x VOUT_DROOP + 10 I_O x VOUT_DROOP + V_O x 10	mV mV

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by the equation fSW = 16MHz/n where $12 \le n \le 80$.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: SYNC pin-strap setting

Units: kHz

Equation: FREQUENCY_SWITCH = $Y \times 2^N$

Range: 615kHz-800kHz

COMMAND	FREQUENCY_SWITCH (33h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	SYNC Pin-strapped Value															

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A desired phase position is specified. Interleave is used for setting the phase offset between individual devices, current sharing groups, and/or combinations of devices and current sharing groups. For devices within single current sharing group the phase offset is set automatically. In a multiphase current share group the same interleave settings must be stored in all devices in the current sharing group in order to phase spread properly. Interleave Offset refers to the phase offset of Phase 0 of the device; Phase 1 is always Phase 0 + 180 degrees.

INTERLEAVE Phase offset is calculated with Equation 6:

$$\text{Phase Offset (in degrees)} = \{\text{Rounded}(\text{Position} \bullet 16/\text{Number})\} \bullet 22.5 \qquad \text{(EQ. 6)}$$

Phase offsets greater than 360 degrees are “wrapped around” by subtracting 360 degrees.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	INTERLEAVE (37h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	Set by CFG Pin-strap Setting															

BITS	PURPOSE	VALUE	DESCRIPTION
15:8	Not Used	0	Not used
7:4	Number In Group	0 to 15d	Sets the number of devices in the interleave group. A value of 0 is interpreted as 16.
3:0	Position in Group (Interleave Order)	0 to 15d	Sets position of the device’s rail within the group. A value of 0 is interpreted as 16. Position 1 will have a 22.5 degree offset.

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the VOUT overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.10 x VSET pin-strap setting.

Units: V

Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT $\times 2^{-13}$

Range: 0V to 7.99V

COMMAND	VOUT_OV_FAULT_LIMIT (40h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.10 x VSET Pin-strap Setting															

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the VOUT overvoltage fault response. The retry time is the time between restart attempts. It's highly recommended set as default "JLPJ = no retry and JLP1J = retry continuously with retry time 280ms" Artesyn qualified only.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: JLPJ = 80h (shut down immediately, no retry)
JLP1J = BFh (Retry continuously, 280ms)

Units: Retry time = 35ms increments

COMMAND	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

<table>
<tr><th>BIT NUMBER</th><th>FIELD NAME</th><th>VALUE</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="2">7:6</td><td rowspan="2">Response behavior, the device:
Pulls SALRT low
Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.</td><td>00-01</td><td>Not used</td></tr>
<tr><td>10-11</td><td>Disable and retry according to the setting in bits [5:3]</td></tr>
<tr><td rowspan="3">5:3</td><td rowspan="3">Retry Setting</td><td>000</td><td>No retry. The output remains disabled until the device is restarted.</td></tr>
<tr><td>001-110</td><td>Not used</td></tr>
<tr><td>111</td><td>Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shutdown. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms</td></tr>
<tr><td>2:0</td><td>Retry Delay</td><td>000-111</td><td>Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.</td></tr>
</table>

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the VOUT under voltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_FAULT_LIMIT should be set to a value below POWER_GOOD

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned.

Type: R/W

Protectable: Yes

Default Value: 0.85 x VSET pin-strap setting.

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT $\times 2^{-13}$

Range: 0V to 7.99

<table>
<tr><th>COMMAND</th><th colspan="16">VOUT_UV_FAULT_LIMIT (44h)</th></tr>
<tr><td>Format</td><td colspan="16">Linear-16 Unsigned</td></tr>
<tr><td>Bit Position</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>Default Value</td><td colspan="16">0.85 x VSET Pin-strap Setting</td></tr>
</table>

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the VOUT under voltage fault response. Note that VOUT UV faults can only occur after Power-good (PG) has been asserted. Under some circumstances this will cause the output to stay fixed below the power-good threshold indefinitely. If this behavior is undesired, use setting 80h. The retry time is the time between restart attempts. It's highly recommended set as default "JLPJ = no retry and JLP1J = retry continuously with retry time 280ms" Artesyn qualified only.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field.

Type: R/W

Protectable: Yes

Default Value: JLPJ = 80h (shut down immediately, no retry)

JLP1J = BFh (Retry continuously, 280ms)

Units: Retry time unit = 35ms

COMMAND	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT NUMBER	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: Pulls SALRT low Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10-11	Disable and retry according to the setting in bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

OT_FAULT_LIMIT (4Fh)

Definition: The OT_FAULT_LIMIT command sets the temperature at which the device should indicate an over-temperature fault.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EBC0h (+120° C)

Units: Celsius

Equation: OT_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 175° C

COMMAND	OT_FAULT_LIMIT (4Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

OT_FAULT_RESPONSE (50h)

Definition: The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over-temperature fault. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: FFh (Continuous retries, retry delay 280ms)

Units: Retry time unit = 35ms

COMMAND	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT NUMBER	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: Pulls SALRT low Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and Retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the temperature falls below the OT_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

OT_WARN_LIMIT (51h)

Definition: The OT_WARN_LIMIT command sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE and notifies the host.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EB70h (+110° C)

Units: Celsius

Equation: OT_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 175° C

COMMAND	OT_WARN_LIMIT (51h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the VIN overvoltage fault threshold. Do not set VIN_OV_FAULT_LIMIT>15.5V, it will damage the module

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D3E0h (15.5V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = Y×2N

Range: 0 to 15.5V

COMMAND	VIN_OV_FAULT_LIMIT (55h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N								Signed Mantissa, Y							
Default Value	1	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the VIN overvoltage fault response as defined by the table below. It's highly recommended set as default "JLPJ = no retry and JLP1J = retry continuously with retry time 280ms" Artesyn qualified only.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: JLPJ = 80h (shut down immediately, no retry)

JLP1J = BFh (Retry continuously, 280ms)

Units: N/A

COMMAND	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT NUMBER	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: Pulls SALRT low Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and Retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the temperature rises above the VIN_OV_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold as defined by the table below. In response to the OV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT and notifies the host.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D3A0h (14.5V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_OV_WARN_LIMIT (57h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the VIN under voltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, Sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CB99 (7.195V)

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_UV_WARN_LIMIT (58h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1.10 x UVLO Pin-strap Setting															

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} under voltage fault threshold.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CB73h(6.898V)

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_UV_FAULT_LIMIT (59h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	UVLO pin-strapped value															

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the VIN under voltage fault response as defined by the table below. The retry time is the time between restart attempts. It's highly recommended set as default "retry continuously with retry time 280ms" Artesyn qualified only.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: BFh (continuous retries, 280ms retry delay)

Units: Retry time unit = 35ms

COMMAND	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT NUMBER	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: Pulls SALRT low Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and Retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the temperature rises above the UT_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shutdown. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT. POWER_GOOD_ON should be set to a value above VOUT_UV_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.9 x VSET pin-strap setting.

Units: V

COMMAND	POWER_GOOD_ON (5Eh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VSET Pin-strap Setting															

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of VOUT rise.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: Vo1= D280h (10ms), Vo2 = CA80h (5ms)

Units: ms

Equation: TON_DELAY = $Y \times 2^N$

Range: 2ms to 5s

COMMAND	TON_DELAY (60h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TON_RISE (61h)

Definition: Sets the rise time of VOUT after ENABLE and TON_DELAY for single and dual channel operation. To adjust the rise time in 4-,6- or 8-phase operation, use MULTI_PHASE_RAMP_GAIN (D5h).
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA80h (5ms)
Units: ms
Equation: TON_RISE = $Y \times 2^N$
Range: 0 to 100ms. Although values can be set below 0.50ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

COMMAND	TON_RISE (61h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of VOUT fall.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: ms

Equation: TON_DELAY = Y×2N

Range: 0 to 5 seconds

COMMAND	TOFF_DELAY (64h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_FALL(65h)

Definition: Sets the fall time for VOUT after DISABLE and TOFF_DELAY. This setting is only valid in single or 2-phase operation. Setting the TOFF_FALL to values less than 0.5ms will cause the LGA50D to turn-off both the high and low-side FETs (or disable the DrMOS device) immediately after the expiration of the TOFF_DELAY time. In 4-, 6- or 8-phase operation, the LGA50D will always turn-off both the high and low-side FETs (or disable the DrMOS device) immediately after the expiration of the TOFF_DELAY time.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: ms

Equation: TON_RISE = $\mathbf{Y \times 2^N}$

Range: 0 to 100ms. Although values can be set below 0.50ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

COMMAND	TOFF_FALL (65h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

STATUS_BYTE (78h)

Definition: The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	None of the above	A fault other than the faults listed in bits 7:1 above has occurred. The source of the fault will be in bits 15:8 of the STATUS_WORD

STATUS_WORD (79h)

Definition: The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Protectable: No

Default Value: 0000h

Units: N/A

COMMAND	STATUS_WORD (79h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current fault has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated. (Note 1)
10	NOT USED	Not used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, or STATUS_MFR_SPECIFIC is set.
8	Not Used	Not used
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	VOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	None of the above	A fault other than the faults listed in bits 7:1 above has occurred. The source of the fault will be in bits 15:8 of the STATUS_WORD

NOTE 1: If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.

STATUS_VOUT (7Ah)

Definition: The STATUS_VOUT command returns one data byte with the status of the output voltage.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_VOUT(7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Not Used
5	VOUT_UV_WARNING	Not Used
4	VOUT_UV_FAULT	Indicates an output under voltage fault.
3:0	Not Used	Not Used

STATUS_IOUT (7Bh)

Definition: The STATUS_IOUT command returns one data byte with the status of the output current.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output over current fault has occurred.
6	Not Used	Not Used
5	Not Used	Not Used
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	Not Used	Not Used

STATUS_INPUT(7Ch)

Definition: The STATUS_INPUT command returns input voltage and input current status information.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	Not Used	Not Used

STATUS_TEMPERATURE (7Dh)

Definition: The STATUS_TEMPERATURE command returns one byte of information with a summary of any temperature related faults or warnings.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_TEMP (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UV_FAULT	An under-temperature fault has occurred.
3:0	Not Used	Not Used

STATUS_CML(7Eh)

Definition: The STATUS_WORD command returns one byte of information with a summary of any communications, logic and/or memory errors.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus™ command was received..
6	The PMBus™ command was sent with invalid or unsupported data.
5	A packet error was detected in the PMBus™ command.
4:2	Not used
1	A PMBus™ command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: The STATUS_MFR_SPECIFIC command returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	MEANING
7	Not Used	Not used
6	DDC Warning	An error was detected on the DDC bus.
5	VMON UV Warning	The voltage on the VMON pin has dropped 10% below the level set by MFR_VMON_UV_FAULT.
4	VMON OV Warning	The voltage on the VMON pin has risen 10% above the level set by MFR_VMON_OV_FAULT.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Not Used	Not used
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by MFR_VMON_UV_FAULT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by MFR_VMON_OV_FAULT.

READ_VIN (88h)

Definition: Returns the input voltage reading.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: V

Equation: READ_VIN = $Y \times 2^N$

Range: N/A

COMMAND	READ_VIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: Read Only

Protectable: No

Default Value: N/A

Equation: READ_VOUT = READ_VOUT $\times$ 2^{-13}

Units: V

COMMAND	READ_VOUT (8Bh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	N/A															

READ_IOUT(8Ch)

Definition: Returns the input current reading.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: A

Equation: READ_IOUT = Y$\times$$2^N$

Range: N/A

COMMAND	READ_IOUT(8Ch)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_TEMPERATURE_1(8Dh)

Definition: Returns the temperature reading internal to the device..

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Equation: READ_TEMPERATURE_1 = $Y \times 2^N$

Range: N/A

COMMAND	READ_TEMPERATURE_1 (8Dh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

Definition: READ_TEMPERATURE_3(8Fh)

Definition: Returns the temperature reading from the DrMOS.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: ^{o}C

Equation: READ_TEMPERATURE_1 = $Y \times 2^{N}$

Range

COMMAND	READ_TEMPERATURE_3 (8Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: %

Equation: READ_DUTY_CYCLE = $Y \times 2^N$

Range: 0 to 100%

COMMAND	READ_DUTY_CYCLE (94h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Default Value: N/A

Units: kHz

Equation: READ_FREQUENCY = $Y \times 2^N$

Range: N/A

COMMAND	READ_FREQUENCY (95h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

PMBus^{TM}_REVISION (98h)

Definition: The PMBus^{TM}_REVISION command returns the revision of the PMBus^{TM} Specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: 22h (Part 1 Revision 1.2, Part 2 Revision 1.2)

Units: N/A

COMMAND	PMBus^{TM}_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	0	0	0	1	0

BIT 7:4	RART 1 REVISION	BITS 3:0	RART 2 REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2

MFR_ID (99h)

Definition: MFR_ID sets a user defined identification string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII, ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: LGA50D-01DADJLPJ/LGA50D-01DADJLP1J

Units: N/A

MFR_REVISION (9Bh)

Definition: MFR_REVISION sets a user defined revision string not to exceed 32 bytes. The sum total of characters in MFR_ID,MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: 002

Units: N/A

MFR_LOCATION (9Ch)

Definition: MFR_LOCATION sets a user defined location identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID,MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_DATE (9Dh)

Definition: MFR_DATE sets a user defined date string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_SERIAL (9Eh)

Definition: MFR_SERIAL sets a user defined serialized identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

USER_DATA_00 (B0h)

Definition: USER_DATA_00 sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes.This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

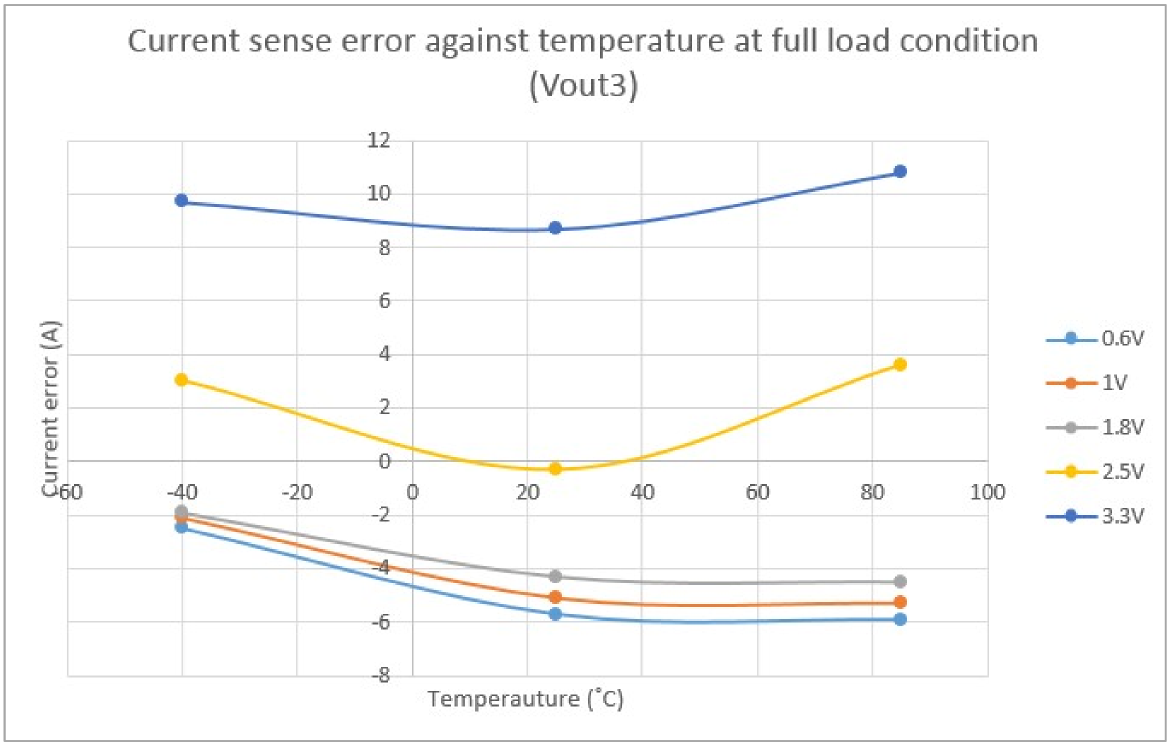
Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

Current Sense Error Against Temperature at Full Load – 2 Phases Single Output



Switching frequency: 0.6Vout -1Vout = 615kHz

1.8Vout-3.3Vout = 800kHz

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command should be saved immediately after being written to the desired user or default store. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	USER_CONFIG (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	CFG Pin-strap Setting															

BIT	FIELD NAME	VALUE	SETTING	Description
15:11	Minimum Duty Cycle	00010	1.17%	Sets the minimum duty-cycle to 2X(VALUE+1)/512. Must be enabled with Bit 7
10	Not Used	1	Not Used	Not Used
9:8	Not Used	00	Not Used	Not Used
7	Minimum Duty Cycle Control	1	Enable	Control for minimum duty cycle
6	Not Used	0	Not Used	Not Used
5	VSET Select	0	VSET0	0 = Uses only VSET0 to set the pin-strapped output voltage
		1	VSET1	1 = Uses only VSET1 to set the pin-strapped output voltage
4	Not Used	0	Not Used	Not Used
3	PWNL disabled state	0	Low when disabled	PWML is low (off) when device is disabled (bit 3 set to 0), or high (on) when device is disabled (bit 3 set to 1)
2	Power-good Configuration	1	Push-Pull	1 = PG is push-pull output

BIT	FIELD NAME	VALUE	SETTING	Description
1	XTEMP Enable	0	Disable	Enable external temperature sensor
0	XTEMP Fault Select	0	Disable	Selects external temperature sensor to determine temperature faults

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing for up to 8 phases. To operate as a 2-phase controller, set both phases to the same rail ID, set phases in rail to 2, then set each phase ID sequentially as 0 and 1. To operate as a 4-phase controller, set all phases to the same rail ID, set phases in rail to 4, then set each phase ID alternately, for example, the first LGA50D will be set to 0 and 2, the second LGA50D will be set to 1 and 3. The LGA50D will automatically equally offset the phases in the rail. Phase spreading is done automatically as part of the DDC_CONFIG command. When using CFG pin-strap settings, the DDC_CONFIG command is set automatically.

NOTE: The output MUST be connected to VSEN0P and VSEN0N when operating as a 2-phase controller.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: PMBus™ address pin-strap dependent.

Units: N/A

COMMAND	DDC_CONFIG (D3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	Description
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (Shared output)
7:3	Not Used	00	00	Not Used
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500ms, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h, 1ms

Units: ms

Equation: POWER_GOOD_DELAY = $Y \times 2^N$

Range: 0 to 500ms

COMMAND	POWER_GOOD_DELAY (D4h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

MULTI_PHASE_RAMP_GAIN (D5h)

Definition: MULTI_PHASE_RAMP_GAIN command value indirectly determines the output voltage rise time during the turn-on ramp. Typical gain values range from 1 to 10. Lower gain values produce longer ramp times. MULTI_PHASE_RAMP_GAIN mode is automatically selected when the ZL8802 is configured to operate in a 4-phase current sharing group. When in MULTI_PHASE_RAMP_GAIN mode, the turn-on ramp up is done with the high bandwidth ASCR control circuitry disabled, resulting in a lower loop bandwidth during start-up ramps. Once POWER_GOOD has been asserted, ASCR circuitry is enabled and the ZL8802 operates normally. When MULTI_PHASE_RAMP_GAIN mode is enabled, soft-off ramps are not allowed (TOFF_FALL is ignored). When the LGA50D is commanded to shutdown, the PWMHO/1 output is tri-stated, turning both the high-side and low-side MOSFETs off, and the PWML0/1 pin is pulled low (DrMOS disabled). Large load current transitions during multiphase ramp-ups will cause output voltage discontinuities. When the phase count is 2; i.e., when the LGA50D is operating standalone, ASCR is enabled at all times and all commands associated with turn-on and turn-off (TON_RISE, TOFF_FALL, Soft-Off) operate normally**.**

Rise time can be calculated using Equation 7:

$$\text{RiseTime} = \text{VOUT\_COMMAND} / \{14 \bullet \text{Input Voltage} \bullet \text{FREQUENCY\_SWITCH (in MHz)} \bullet \text{MULTI\_PHASE\_RAMP\_GAIN}\} \quad \text{(EQ. 7)}$$

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Custom

Type: R/W

Protectable: Yes

Default Value: 03h

Units: N/A

COMMAND	MULTI_PHASE_RAMP_GAIN (D5h)							
Format	1 Byte Binary							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	Description
7:0	Gain	00-FF	00	Start-up ramp gain

SNAPSHOT_FAULT_MASK (D7h)

Definition: Prevents faults from causing a SNAPSHOT event (and store) from occurring.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: NA

Range: NA

COMMAND	SNAPSHOT_FAULT_MASK (D7h)															
Format	**Bit Field**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	STATUS BIT NAME	MEANING
15:14	Not Used	Not Used
13	Group	Ignore Fault Spreading faults
12	Phase	Ignore Other Phase faults
11	CPU	Ignore CPU faults
10	CRC	Ignore CRC Memory faults
9	Not Used	Not used
8	Not Used	Not Used
7	IOUT_UC_FAULT	Ignore output undercurrent faults
6	IOUT_OC_FAULT	Ignore output overcurrent faults
5	VIN_UV_FAULT	Ignore input undervoltage faults
4	VIN_OV_FAULT	Ignore Input undervoltage faults
3	UT_FAULT	Ignore under-temperature faults
2	OT_FAULT	Ignore over-temperature faults
1	VOUT_UV_FAULT	Ignore output undervoltage faults
0	VOUT_OV_FAULT	Ignore output overvoltage faults

MFR_SMBALERT_MASK (DBh)

Definition: The MFR_SMBALERT_MASK command is used to prevent faults from activating the SALRT pin. The bits in each byte correspond to a specific fault type as defined in the STATUS command.

Data Length in Bytes: 7

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00 00 00 00 00 00 00h (No faults masked)

Units: N/A

COMMAND	OVUV_CONFIG (DBh)							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Bit Position	55	54	53	52	51	50	49	48
Default Value Byte 6	0	0	0	0	0	0	0	0
Bit Position	47	46	45	44	43	42	41	40
Default Value Byte 5	0	0	0	0	0	0	0	0
Bit Position	39	38	37	36	35	34	33	32
Default Value Byte 4	0	0	0	0	0	0	0	0
Bit Position	31	30	29	28	27	26	25	24
Default Value Byte 3	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value Byte 2	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8
Default Value Byte 1	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value Byte 0	0	0	0	0	0	0	0	0

BIT	STATUS BIT NAME	MEANING
6	STATUS_MFR_SPECIFIC	Mask manufacturer specific faults as identified in the STATUS_MFR_SPECIFIC byte.
5	STATUS_OTHER	Not used
4	STATUS_CML	Mask communications, memory or logic specific faults as identified in the STATUS_CML byte.
3	STATUS_TEMPERATURE	Mask temperature specific faults as identified in the STATUS_TEMPERATURE byte
2	STATUS_INPUT	Mask input specific faults as identified in the STATUS_INPUT byte
1	STATUS_IOUT	Mask output current specific faults as identified in the STATUS_IOUT byte
0	STATUS_VOUT	Mask output voltage specific faults as identified in the STATUS_VOUT byte

PINSTRAP_READ_STATUS (DDh)

Definition: Reads back 7 bytes of 8 bit values that represent the pin-strap settings of each of the device's pin-strap pins. This value corresponds to a resistor value, a high, a low or an open condition. The pin decode values correspond to pin-strap settings according to:

R (kΩ)	DECODE
10	00
11	01
12.1	02
13.3	03
14.7	04
16.2	05
17.8	06
19.6	07
21.5	08
23.7	09
26.1	0A
28.1	0B
31.6	0C
34.8	0D
38.3	0E
42.2	0F
46.4	10

R (kΩ)	DECODE
51.1	11
56.2	12
61.9	13
68.1	14
75	15
82.5	16
90.9	17
100	18
110	19
121	1A
133	1B
147	1C
162	1D
178	1E
LOW	F1
OPEN	F2
HIGH	F3

Paged or Global: Global

Data Length in Bytes: 7

Data Format: Bit Field

Type: Read Only

Protectable: Yes

Default Value: Pin-strap settings

Units: N/A

COMMAND	READ_PINSTRAP (DDh)							
Format	Bit Field							
Access	R	R	R	R	R	R	R	R
Bit Position	55	54	53	52	51	50	49	48
Function	ASCRCFG Pin Decode							
Default Value	ASCRCFG Pin-strap Setting							
Bit Position	47	46	45	44	43	42	41	40
Function	CFG Pin Decode							
Default Value	CFG Pin-strap Setting							
Bit Position	39	38	37	36	35	34	33	32
Function	SYNC Pin Decode							
Default Value	SYNC Pin-strap Setting							
Bit Position	31	30	29	28	27	26	25	24
Function	UVLO Pin Decode							
Default Value	UVLO Pin-strap Setting							
Bit Position	23	22	21	20	19	18	17	16
Function	VSET0 Pin Decode							
Default Value	VSET0 Pin-strap Setting							
Bit Position	15	14	13	12	11	10	9	8
Function	VSET1 Pin Decode							
Default Value	VSET1 Pin-strap Setting							
Bit Position	7	6	5	4	3	2	1	0
Function	Reserved							
Default Value	N/A							

BIT	FIELD NAME	VALUE	Description
55:48	ASCRCFG Pin Decode	00-F4h	Decode value of ASCRCFG pin-strap setting
47:40	CFG Pin Decode	00-F4h	Decode value of CFG pin-strap setting
39:32	SYNC Pin Decode	00-F4h	Decode value of SYNC pin-strap setting
31:24	UVLO Pin Decode	00-F4h	Decode value of UVLO pin-strap setting
23:16	VSET0 Pin Decode	00-F4h	Decode value of VSET0 pin-strap setting
15:8	VSET1 Pin Decode	00-F4h	Decode value of VSET1 pin-strap setting
7:0	Not Used	FF	Not used

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain and residual value are automatically set by the LGA50D based on input voltage and output voltage. ASCR gain is analogous to bandwidth, ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but will not affect the peak output voltage deviation. Typical ASCR gain settings range from 100 to 800, and ASCR residual settings range from50 to 90. it is recommended to set ASCR gain to 200 and ASCR residual to 90 with recommended output capacitor in “Output Specifications” section. It is also recommended to follow “PCB layout Guideline” for stability. If customer need to reset the ASCR_CONFIG, customer need to check the stability with the new ASCR_CONFIG setting base on their application. In multi - phase condition, the ASCR setting must be set the same for all phases. For 6 phases and 8 phases, the ASCR_CONFIG is set by PMBUS command.

Paged or Global: Paged

Data Length in Bytes: 4

Data Format: Bit Field and nonsigned binary

Type: R/W

Protectable: Yes

Default Value: ASCRCFG pin-strap setting

Units: N/A

COMMAND	ASCR_CONFIG (DFh)							
Format	Bit Field/Linear-8 Unsigned							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Position	31	30	29	28	27	26	25	24
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value	ASCRCFG Pin-strap Setting (residual)							
Format	Linear-16 Unsigned							
Bit Position	15	14	13	12	11	10	9	8
Function	See Following Table							
Default Value	ASCRCFG Pin-strap Setting (gain)							
Bit Position	7	6	5	4	3	2	1	0
Function	See Following Table							
Default Value	ASCRCFG Pin-strap Setting (gain)							

BITS	PURPOSE	VALUE	Description
31:25	Not Used	0000000h	Not used
24	ASCR Enable	1	Enable
23:16	ASCR Residual Setting	0 - 7Fh	ASCR residual
7:0	ASCR Gain Setting	0-FF	ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multirail sequencing. The device will enable its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus as a result of the prequel's Power-good (PG) signal going high. The device will disable its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus at the completion of its ramp-down (its output voltage is 0V). The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (prequel and sequel disabled)

Units: N/A

COMMAND	SEQUENCE (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	Description
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail
		1	Enable	Enable, prequel to this rail is defined by bits 12:8
14:13	Not Used	0	Not Used	Not Used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable, no sequel following this rail
		1	Enable	Enable, sequel to this rail is defined by bits 4:0
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31D	DDC ID	Set to the DDC ID of the sequel rail

DDC_GROUP (E2h)

Definition: Rails (output voltages) are assigned Group numbers in order to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that DDC Groups are separate and unique from DDC Rail IDs (see “DDC_CONFIG (D3h)” section. Current sharing rails need to be in the same DDC Group in order to respond to broadcast VOUT_COMMAND and OPERATION commands. Power fail event responses (and phases) are automatically spread in Phase 0 and 1 when the LGA50D is operating in 2-phase current sharing mode when it is configured using DDC_CONFIG, regardless of its setting in DDC_GROUP.

Paged or Global: Paged

Data Length in Bytes: 34

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	DDC_GROUP (E2h)							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Position	31	30	29	28	27	26	25	24
Function	Not Used							
Bit Position	23	22	21	20	19	18	17	16
Format	Bit Field		EN>	VOUT_COMMAND Group ID				
Default Value	Set by CFG Pin-strap Setting							
Bit Position	15	14	13	12	11	10	9	8
Function	Not Used		EN>	OPERATION Group ID				
Default Value	Set by CFG Pin-strap Setting							
Bit Position	7	6	5	4	3	2	1	0
Function	Not Used		EN>	Power Fail Group ID				
Default Value	Set by CFG Pin-strap Setting							

BITS	PURPOSE	VALUE	Description
31:22	Not Used	00	Not used
21	BROADCAST_VOUT_COMMAND response	1	Responds to broadcast VOUT_COMMAND with same Group ID
		0	Ignores broadcast VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events
15:14	Not Used	00	Not Used
13	BROADCAST_OPERATION response	1	Responds to broadcast OPERATION with same Group ID
		0	Ignores broadcast OPERATION
12:8	BROADCAST_OPERATION group ID	0-31d	Group ID sent as data for broadcast OPERATION events
7:6	Not Used	00	Not used
5	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID by shutting down immediately
		0	Responds to POWER_FAIL events with same Group ID with sequenced shutdown
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the IOUT overcurrent fault response as defined by the table below. The command format is the same as the PMBus™ standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts. It's highly recommended set as default "JLPJ = no retry and JLP1J = retry continuously with retry time 280ms" Artesyn qualified only.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: JLPJ = 80h (shut down immediately, no retry)

JLP1J = BFh (Retry continuously, 280ms)

Units: Retry time unit = 35ms

COMMAND	MFR_IOUT_OC_FAULT_RESPONSE (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	Description
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault is no longer present.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the IOUT undercurrent fault response as defined by the table below. The command format is the same as the PMBus™ standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts. It's highly recommended set as default "JLPJ = no retry and JLP1J = retry continuously with retry time 280ms" Artesyn qualified only.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: JLPJ = 80h (shut down immediately, no retry)

JLP1J = BFh (Retry continuously, 280ms)

Units: Retry time unit = 35ms

COMMAND	MFR_IOUT_UC_FAULT_RESPONSE (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	Description
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault is no longer present.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the IOUT average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (inSTATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 27A

Units: Amperes

Equation: IOUT_AVG_OC_FAULT_LIMIT = $Y \times 2^N$

Range: 0A-27A

COMMAND	IOUT_AVG_OC_FAULT_LIMIT (E7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	CFG Pin-strap Setting															

USER_GLOBAL_CONFIG (E9h)

Definition: This command is used to set options for output voltage sensing, VMON/TMON pin configuration, SMBus time-out and DDC and SYNC output configurations..

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	USER_GLOBAL_CONFIG (E9h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	Set by CFG Pin-strap Setting															

BIT	FIELD NAME	VALUE	Description
15:13	Not Used	000000	Not used
12	VMON/TMON Config	1	READ_TEMPERATURE_3 returns TMON in ° C. External 2:1 voltage divider needed on VMON/TMON pin (pin 6) to SPS TMON pin.
11:10	Not Used	00	Not used
9:8	VSENSE Select for monitoring and fault detection	00	Output 0 uses VSEN0, Output 1 uses VSEN1
		01	Both outputs use VSEN0
		10-11	Not used
7	Not Used	0	Not used
6	DDC output Configuration	0	DDC output open drain
5	Not Used	0	Not Used
4	Disable SMBus Time-Outs	0	SMBus time-outs enabled
3	Not Used	0	Not Used
2:1	Sync I/O Control	00	Use internal clock (frequency initially set with pin-strap)
		01	Use internal clock and output internal clock (not for use with pin-strap)
0	Not Used	0	Not used

SNAPSHOT (EAh)

Definition: The SNAPSHOT command is a 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or via a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT. Because there is a fault stored in SNAPSHOT already during Artesyn factory qualification test, please erase it firstly before using SNAPSHOT function.

Paged or Global: Paged

Data Length in Bytes: 32

Data Format: Bit Field

Type: Block Read

Protectable: No

Default Value: N/A

Units: N/A

BIT	VALUE	PMBus™ COMMAND	FORMAT
31:23	Not Used	Not Used	0000h
22	Flash Memory Status Byte	N/A	Bit Field
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	IOUT Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	VOUT Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
11:10	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
7:6	Highest Measured Output Current	N/A	2 Byte Linear-11
5:4	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
3:2	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
1:0	Input Voltage	READ_VIN (88h)	2 Byte Linear-11

LEGACY_FAULT_GROUP (F0h)

Definition: This command allows the LGA50D to sequence and fault spread with devices other than the ZL8800 family of ICs. This command sets which rail DDC IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

NOTE: The device/rail's own DDC ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail.

All devices in a current share rail (devices other than the ZL8800 family ICs) must shut down for the rail to report a shutdown. If fault spread mode is enabled in USER_CONFIG, the device will immediately shut down if on of its DDC_GROUP members fail. The device/rail will attempt its configured restart only after all devices/rails within the DDC_GROUP have cleared their faults. If fault spread mode is disabled in USER_CONFIG, the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the DDC_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Data Length in Bytes: 4

Data Format: Bit field

Type: Block R/W

Protectable: Yes

Default Value: 00000000h

Units: N/A

COMMAND	LEGACY_FAULT_GROUP (F0h)							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Position	31	30	29	28	27	26	25	24
Default Value	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0
Function	See Following Table							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Position	15	14	13	12	11	10	9	8
Default Value	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0
Function	See Following Table							

BITS	PURPOSE	SETTING	Description
31:0	Fault Group	00000000h	Identifies the devices in the fault spreading group.

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h will cause the device to copy the current SNAPSHOT values from NVRAM to the 32-byte SNAPSHOT command parameter. Writing a 02h will cause the device to write the current SNAPSHOT values to NVRAM, 03h will erase all SNAPSHOT values from NVRAM. Write (02h) and Erase (03h) may only be used when the device is disabled. All other values will be ignored. SNAPSHOT03h must be written to the device when the device is DISABLED. Data will not be updated, or written to NVRAM after a fault occurs until the SNAPSHOT 03h command has been written.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W Byte

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	SNAPSHOT_CONTROL (F3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	DESCRIPTION
01	Read SNAPSHOT values from NVRAM
02	Write SNAPSHOT values to NVRAM
03	Erase SNAPSHOT values from NVRAM

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write Only

Protectable: Yes

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Sets the VMON over-temperature fault threshold. The VMON overvoltage warn limit is automatically set to 90% of this fault value. If VMON is not used, set VMON_OV_FAULT_RESPONSE to 00h, which will disable VMON OV faults entirely.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: C266h (2.4V)

Units: Volts

Equation: MFR_VMON_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 20V

COMMAND	MFR_VMON_OV_FAULT_LIMIT (F5h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Sets the VMON under voltage fault threshold. The VMON undervoltage warn limit is automatically set to 110% of this fault value. If VMON is not used, set VMON_UV_FAULT_RESPONSE to 00h, which will disable VMON UV faults entirely.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 9B33h (0.1V)

Units: Volts

Equation: MFR_VMON_UV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 20V

COMMAND	MFR_VMON_UV_FAULT_LIMIT (F6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0

MFR_READ_VMON (F7h)

Definition: Reads the voltage on the VMON pin.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: ° C

Equation: MFR_READ_VMON = Y x 2^N

Range: -200° C to +200° C

COMMAND	MFR_READ_VMON (F7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

VMON_OV_FAULT_RESPONSE (F8h)

Definition: Configures the VMON overvoltage fault response as defined by the table below. Note: The retry time is the time between restart attempts. If VMON is not used, set this response to 00h, which will disable VMON OV faults entirely

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: BFh (continuous retries)

Units: N/A

COMMAND	VMON_OV_FAULT_RESPONSE (F8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT	FIELD NAME	VALUE	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Ignore faults
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault is no longer present.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after VMON falls below 95% of the VMON_OV_FAULT_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VMON_UV_FAULT_RESPONSE (F9h)

Definition: Configures the VMON under voltage fault response as defined by the table below. Note: The retry time is the time between restart attempts. If VMON is not used, set this response to 00h, which will disable VMON UV faults entirely

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field.

Type: R/W

Protectable: Yes

Default Value: BFh (continuous retries)

Units: Retry time unit = 35ms

COMMAND	VMON_UV_FAULT_RESPONSE (F9h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT	FIELD NAME	VALUE	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Ignore faults
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault is no longer present.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after VMON falls below 95% of the VMON_OV_FAULT_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

SECURITY_LEVEL (FAh)

Definition: The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writeable (commands are always readable). If a command is not writeable, a password must be entered in order to change its parameter (i.e., to enable writes to that command). There are two types of passwords, public and private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as no writeable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as no writeable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT store must be sent in order to change that command. If a command is writeable according to the default UNPROTECT parameter, it may still be marked as non-writeable in the user store UNPROTECT parameter. In this case, the user private password can be sent to make the command writeable. The device supports four levels of security. Each level is designed to be used by a particular class of users, ranging from module manufacturers to end users, as discussed below. Levels 0 and 1 correspond to the public password. All other levels require a private password. Writing a private password can only raise the security level. Writing a public password will reset the level down to 0 or 1.

Figure 58 shows the algorithm used by the device to determine if a particular command write is allowed.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Hex

Type: Read Byte

Protectable: No

Default Value: 01h

Units: N/A

LGA50D set security level to 1 that protect Artesyn default settings via a password.

User can save their settings in user store via PMBus^{TM} command STORE_USER_ALL that is in effect on LGA50D.

User cannot overwrite Artesyn's default settings without correct password.

User can restore to Artesyn's default settings via send below PMBus^{TM} commands one by one, after recycle Vin, LGA50D settings are back to Artesyn's default settings.

1.PRIVATE_PASSWORD (send null string 000000000000000000h)

2.RESTORE_FACTORY

3.PRIVATE_PASSWORD (send null string 000000000000000000h)

4.STORE_USER_ALL

5. Recycle Vin

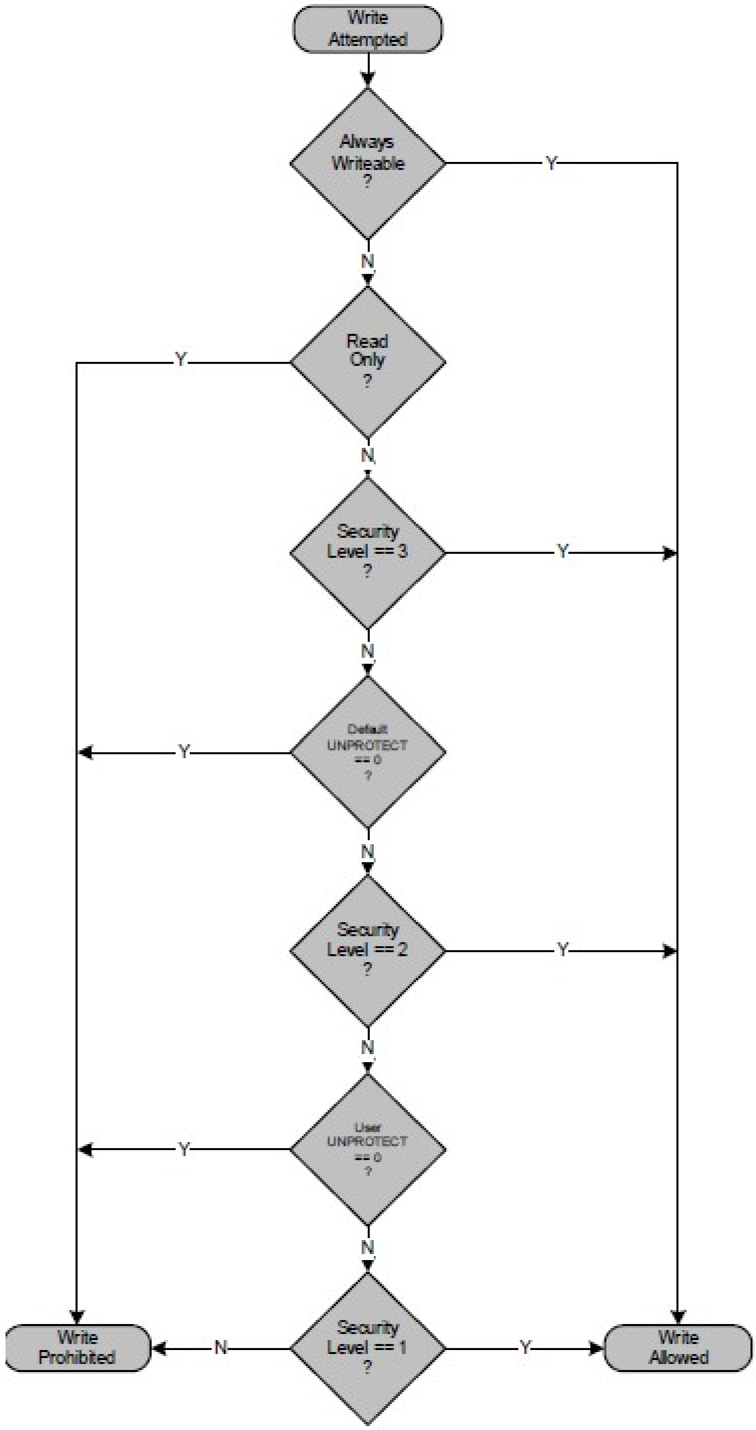


Figure 58 ALGORITHM USED TO DETERMINE WHEN A COMMAND IS WRITEABLE

Security Level 3 - Module Vendor

Level 3 is intended primarily for use by module vendors to protect device configurations in the default store. Clearing a UNPROTECT bit in the default store implies that a command is writeable only at Level 3 and above. The device's security level is raised to Level 3 by writing the private password value previously stored in the default store. To be effective, the module vendor must clear the UNPROTECT bit corresponding to the STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 3 protection is ineffective since the entire store could be replaced by the user, including the enclosed private password.

Security Level 2 - User

Level 2 is intended for use by the end user of the device. Clearing a UNPROTECT bit in the user store implies that a command is writeable only at Level 2 and above. The device's security level is raised to Level 2 by writing the private password value previously stored in the User Store. To be effective, the user must clear the UNPROTECT bit corresponding to the STORE_USER_ALL, RESTORE_DEFAULT_ALL, STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 2 protection is ineffective since the entire store could be replaced, including the enclosed private password.

Security Level 1 - Public

Level 1 is intended to protect against accidental changes to ordinary commands by providing a global write-enable. It can be used to protect the device from erroneous bus operations. It provides access to commands whose UNPROTECT bit is set in both the default and User Store. Security is raised to Level 1 by writing the public password stored in the user store using the PUBLIC_PASSWORD command. The public password stored in the default store has no effect.

Security Level 0 - Unprotected

Level 0 implies that only commands which are always writeable (e.g., PUBLIC_PASSWORD) are available. This represents the lowest authority level and hence the most protected state of the device. The level can be reduced to 0 by using PUBLIC_PASSWORD to write any value which does not match the stored public password.

PRIVATE_PASSWORD (FBh)

Definition: Sets the private password string.

Paged or Global: Global

Data Length in Bytes: 9

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: No

Default Value: 000000000000000000h

Units: N/A

PUBLIC_PASSWORD (FCh)

Definition: Sets the public password string.

Paged or Global: Global

Data Length in Bytes: 4

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: No

Default Value: 00000000h

Units: N/A

Application Notes

Electrical Description

The LGA50D is designed with a voltage mode dual-phase synchronous buck topology and the block diagram is shown in Figure 59.

The output voltage is adjustable over a range of 0.6 - 3.3V by using an external resistor or PMBus™.

The POL module can be shut down via the ON/OFF input pin. The module is enabled when the ON/OFF pin is in logic high, and disabled when it is in logic low.

The power good signal is an pull up output that is pulled low by the PWM controller when it detects the output exceeded ±10% of the set value.

The output is monitored for over current and short-circuit conditions. When the PWM controller detects an over current condition, it forces the module into the defaulted latch mode.

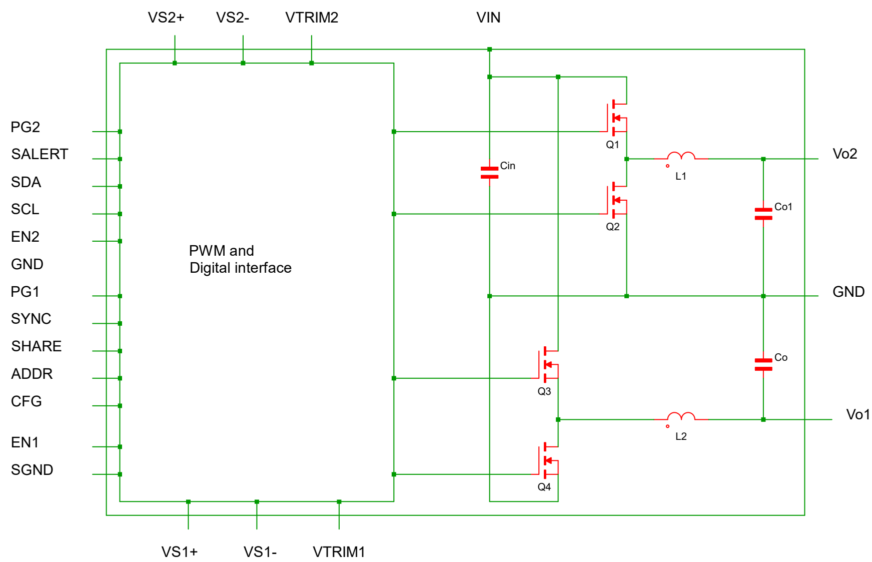


Figure 59: Electrical Block Diagram

Wide Operating Temperature Range

The LGA50D's ability to accommodate a wide range of ambient temperatures is the result of its extremely high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal management within the unit means that it can cover a vast array of applications.

Typical Applications

The LGA50D has a lot of applications. Below are some typical applications:

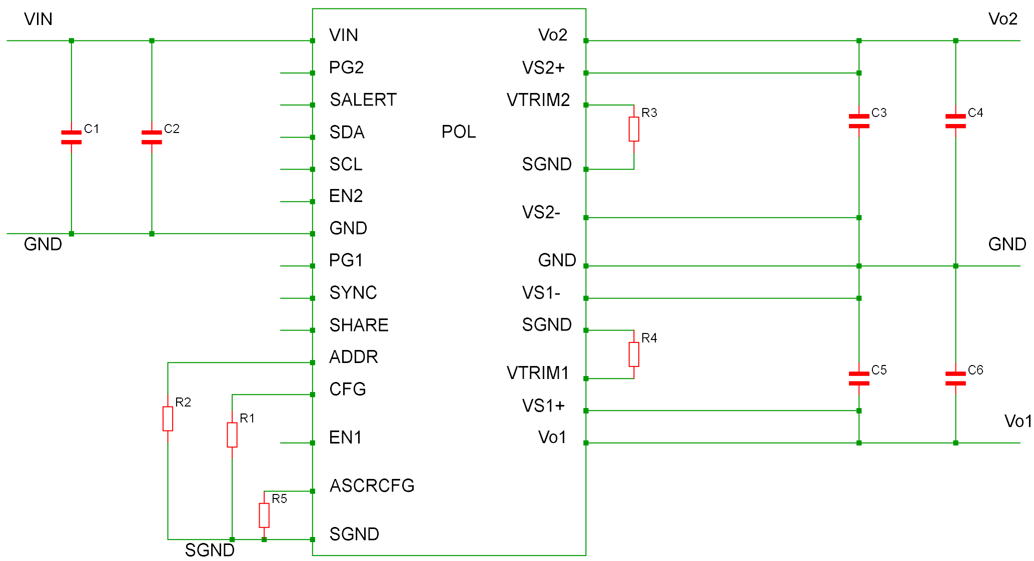


Figure 60: Standard Application

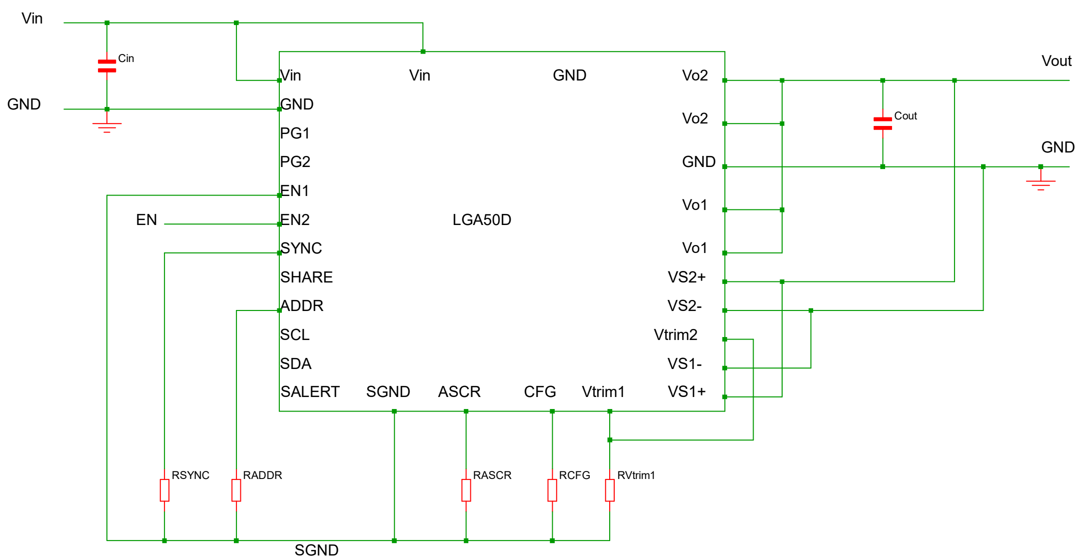


Figure 61: One module one output

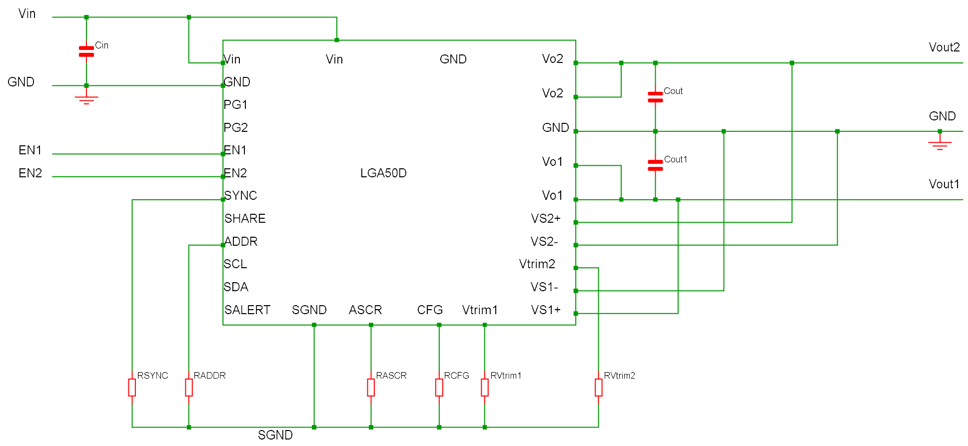


Figure 62: One module two output

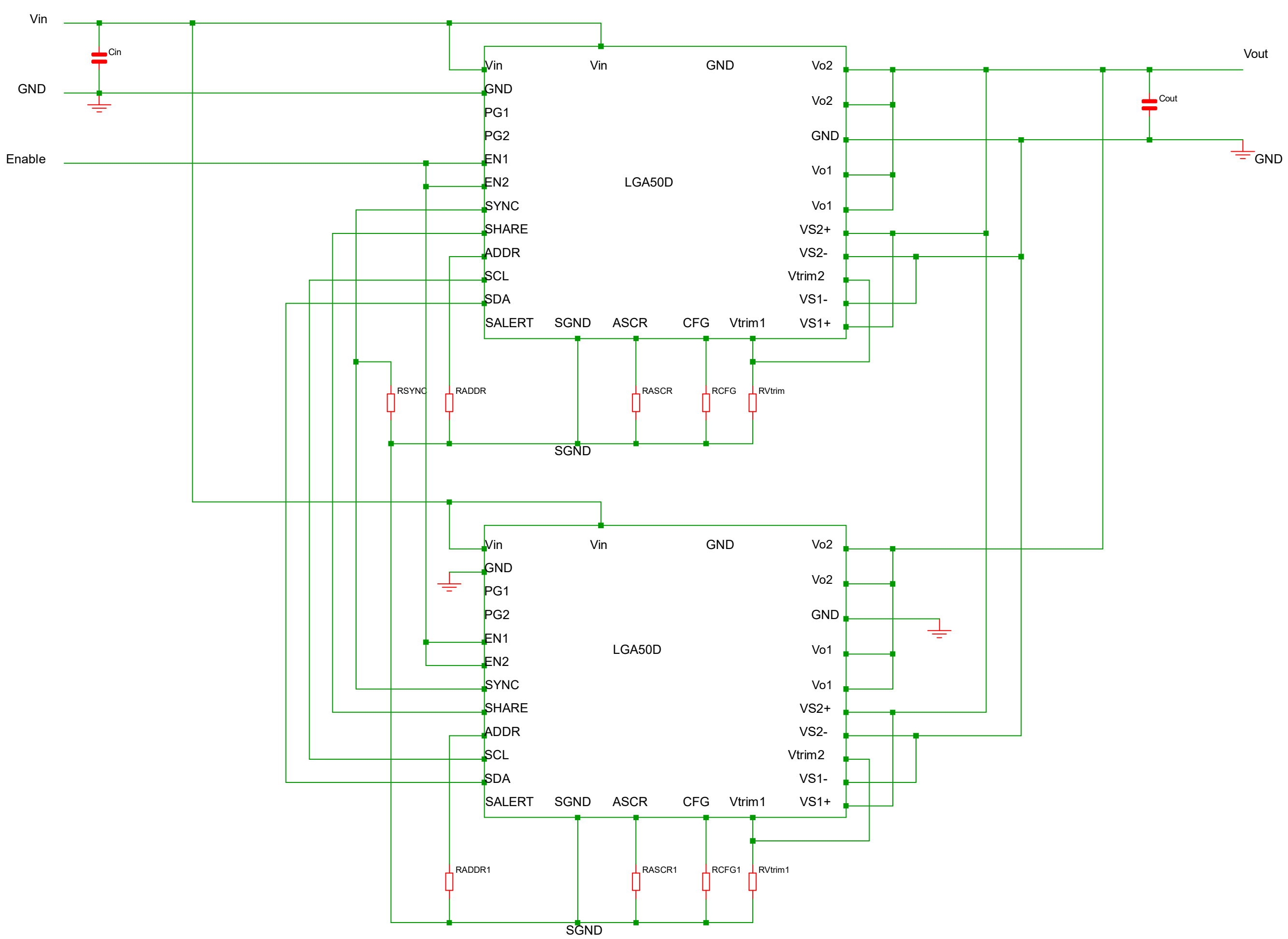
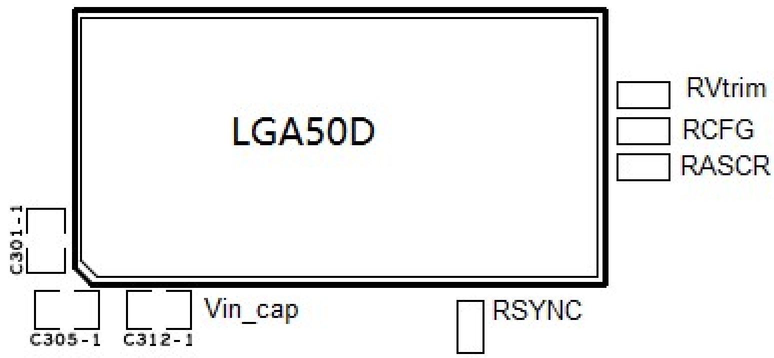


Figure 63: Two modules one output

PCB layout Guideline

1.All the pin strapped resistors, RSYNC, RADDR, RASCR, RVtrim, RCFG, should be placed as close to the LGA50D module pins as possible to minimize loops that may pick up noise. The connection from the Vtrim pin, to the Vtrim resistor, back to SGND must be as short as possible. It is recommended the path including the resistor body should less than 10mm.

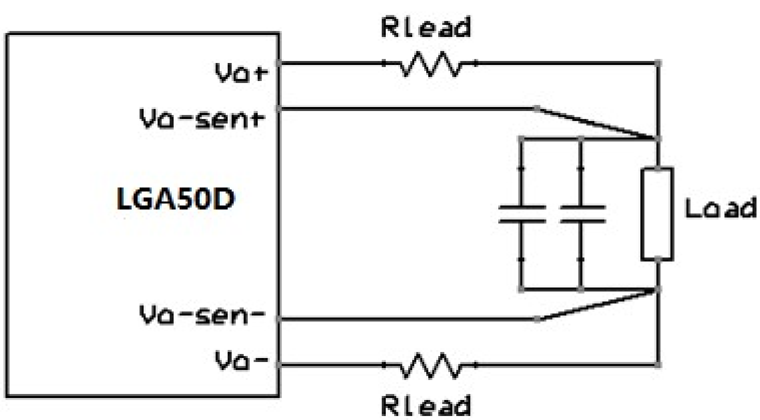


2.The output capacitors should be placed as close to the LGA50D module pins as possible to minimize the output impedance. The output capacitors should also be placed close to the remote sense point for stability.

3.The input ceramic capacitors should be placed as close to the LGA50D module pins as possible to decouple noise.

4.The LGA50D POL modules should be placed closely to the ASIC for better performance. Since the overshoot voltage during step is followed V=L*di/dt, the L is the PCB power trace inductance, if PCB impedance is high, the overshoot voltage may be high.

5.Remote sense VS+, VS- traces should be in paralleled connect to output, the traces are shield by GND to minimized noise couple. Recommended connect VS+/VS- to one high capacitance output capacitor's soldering pads that is close to actual load, please do not connect VS+/VS- very close to LGA50D output pins that is high ripple noise cause control loop unstable.



6.Full hole vias are very helpful for lower impedance and better thermal conductivity. Recommended add 12pcs full hole vias on each power pin soldering pad if possible, such as Vin, Vo, GND. Recommended add 3pcs full hole vias on each soldering pad of output polymer Tan capacitor, add 2pcs full hole vias on each soldering pad of output ceramic capacitor. Even for signal pins, more full hole vias on soldering pads shall improve thermal conductivity that cool down the LGA50D module as well.

Output Voltage Adjustment

The output voltage is adjustable from 0.6V to 3.3V. The outputs can be adjusted with an external resistor placed between the “Vtrim1 or Vtrim2” and “GND” pin shown Figure 64. V_{o1} and V_{o2} can also be set by PMBus™ command. VOUT_MAX is also determined by this pin-strap setting, and is 15% greater than the V_{trim0} and V_{trim1} voltage settings by default, however VOUT_MAX can be changed via the PMBus™. For dual outputs condition, the switching frequency of both outputs must be the same. Also, must use the higher switching frequency between the 2 outputs. For example, if Vout1 = 0.6V and Vout2= 3.3V, the switching frequency for both outputs must be set to 800kHz.

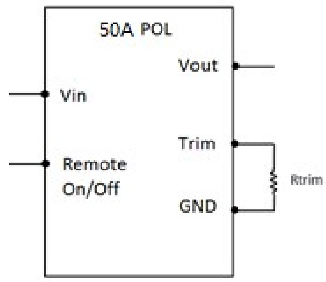


Figure 64: Output Voltage Adjustment

Table 6. Output Voltage Adjustment Reference:

RVSET(kΩ)	VOUT(V)	RVSET(kΩ)	VOUT(V)
LOW	1	38.3	1.3
OPEN	1.2	42.2	1.4
HIGH	0.9	46.4	1.5
10	0.6	51.1	1.6
11	0.65	56.2	1.7
12.1	0.7	61.9	1.8
13.3	0.75	68.1	1.9
14.7	0.8	75	2
16.2	0.85	82.5	2.1
17.8	0.9	90.9	2.2
19.6	0.95	100	2.3
21.5	1	110	2.5
23.7	1.05	121	2.8
26.1	1.1	133	3
28.7	1.15	147	3.3
31.6	1.2	-	-
34.8	1.25	-	-

Module Address Selection

When communicating with multiple SMBus modules using the SMBus interface, each module must have its own unique address so the host can distinguish between the modules. The module address can be set according to the pin-strap options listed in blew table. When operating in 2 output mode, care must be taken when using sequential PMBus™ addresses. Since share addresses are automatically set using the PMBus™ address, it is possible for a module with a PMBus™ address immediately after a 2 output LGA50D module to be automatically configured with the same share address as one of the LGA50D channels, which could cause unintended operating modes. When using the LGA50D in a 4-phase application, the master device address must be 1 higher than the slave address. For this reason, do not use the next higher PMBus™ address when using the LGA50D as a 2 output module. The SMBus address cannot be changed with a PMBus™ command.

Table 7. Module Address Selection Reference:

RSA(kΩ)	SMBus ADDRESS	RSA(kΩ)	SMBus ADDRESS
LOW	40h	42.2	51h
OPEN	42h	46.4	52h
10	41h	51.1	53h
11	43h	56.2	54h
12.1	44h	61.9	55h
13.3	45h	68.1	56h
14.7	46h	75	57h
16.2	47h	82.5	58h
17.8	48h	90.9	59h
19.6	49h	100	5Ah
21.5	4Ah	110	5Bh
23.7	4Bh	121	5Ch
26.1	4Ch	133	5Dh
28.7	4Dh	147	5Eh
31.6	4Eh	162	5Fh
34.8	4Fh	178	60h

Switching Frequency Setting (SYNC)

The LGA50D switching frequency can be set from 615kHz to 800kHz by using the pin-strap method as shown in Table 8, or by using a PMBus™ command. The default switching frequency is set at 800kHz.

The LGA50D incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source. By default, the SYNC pin is configured as an input. The LGA50D will automatically check for a clock signal on the SYNC pin each time EN is asserted. The LGA50D will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 615kHz to 800kHz and must be stable when the EN pin (EN1,EN2) is asserted. When using an external clock, the frequencies are not limited to discrete values as when using the internal clock. The external clock signal must not vary more than 10% from its initial value, and should have a minimum pulse width of 150ns. In the event of a loss of the external clock signal, the output voltage may show transient over shoot or undershoot. If loss of synchronization occurs, the LGA50D will automatically switch to its internal oscillator and switch at its programmed frequency.

The SYNC pin can also be configured as an output. The module will run from its internal oscillator and will drive the SYNC pin so other modules can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode. The switching frequency can be set to any value between 615kHz to 800kHz using a PMBus™ command. The available frequencies below 800kHz are defined by f_{SW} = 16MHz/N, where $20 \leq N \leq 40$.

If a value other than f_{SW} = 16MHz/N is entered using a PMBus™ command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810kHz is entered, the module will select 800kHz (N=20).

Table 8. Switching Frequency Setting Reference:

RSYNC(kΩ)	FREQ(kHz)
31.6	615
34.8	727
38.3	800

EN

EN are used to enable and disable each channel of the LGA50D. The enable pins should be held low whenever a configuration file or script is used to configure the LGA50D, or a PMBus™ command is sent that could potentially damage the application circuit. When the LGA50D is used in a self-enabled mode, for example, when EN1 or EN2 is tied to a external 5Vcc or a resistor divider to VIN, the user must consider the LGA50D's default factory settings. When a configuration file is used to configure the LGA50D, the factory default settings are restored to both the user and default stores in order to set the LGA50D to an initialized state. Since the default state of the LGA50D is to be enabled when the enable pin is high, it is possible for the LGA50D to be enabled while the PMBus™ commands are sent to the LGA50D during the configuration process.

The Enable pin is edge triggered to achieve fast turn-off times. As a result, minimum Enable high and Enable low pulse widths must be observed to ensure correct operation. The minimum high and low pulse widths are dependent on the configured rise, fall and delay times and can be calculated using Equations 1 and 2:

EN low > TOFF_DELAY + TOFF_FALL + 10.5ms (EQ.1)

EN high > TON_DELAY + TON_RISE + POWER_GOOD_DELAY + 5.5ms (EQ.2)

EN low and EN high times shorter than these minimums may result in the device not responding to the trailing edge of the pulse. For example, a EN low pulse below the EN low minimum pulse width may stay in the OFF state until a valid EN low pulse is applied to the EN pin.

The enable signal must be a clean signal with no bouncing. If a physical switch is to be used for enable of the LGA50D, a debounce circuit must be used to ensure EQ.1 and EQ.2 are met.

Power Good

The LGA50D provides a power good signal(PG1, PG2) for each channel that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within 10% of the target voltage.

Digital Bus (Share)

The Digital-DC Communications (Share) bus is used to communicate between modules, and within the LGA50D itself.

This dedicated bus provides the communication channel between modules for features such as sequencing, fault spreading, and current sharing.

The share pin on all Digital-DC modules that utilize sequencing, fault spreading or current sharing must be connected together. The share pin on all Digital-DC modules in an application should be connected together.

Stackable

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each module such that not all modules have coincident rising edges. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses are reduced.

In order to enable stackable feature, all converters must be synchronized to the same switching clock. Configuring the SYNC pin is described in the Configurable Pins Section of this document.

User can set 6 or 8 phases configuration either by Artesyn GUI or PMBus™ commands. Please contact Artesyn to get 6 or 8 phases setting instruction.

.Fault Spreading

The Digital POL modules can be configured to broadcast a fault event over the share bus to the other modules in the group. When a fault occurs and the module is configured to shut down on a fault, the module will shut down and broadcast the fault event over the share bus. The other modules on the share bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Active Current Sharing

The PWM outputs of the LGA50D are used in parallel to create a dual phase power rail. The module outputs will share the current equally within a few percent, assuming all external sensing element variations and tolerances are negligible.

Start-up and shut-down delay characteristics

T-ON delay

The default T-on delay for 2 o/p configuration on LGA50D is

EN1 5ms

EN2 10ms

There is a minimum of 2ms pre-ramp delay between the enable signal and the start of the output voltage ramp. The T-on delay should be set higher than 2ms.

As the controller program is running for individual channel control, it is not able to ensure whether it reads EN1 status or EN2 status first. The turn-on sequencing between EN1 and EN2 can't be guaranteed for the same Ton delay. Therefore the delay is set on both EN1 and EN2 channels. With this setting, the controller can ensure the timing and sequencing on Vo1 and Vo2.

If an application demands both of Vo1 and Vo2 to reach the regulated point at the same time, it is recommended to compensate for this off-set in time by setting Ton rise time appropriately instead of Ton delay.

For reference:

Typical total delays at Vo1 = Ton delays from EN1 + Ton rise delays = 5ms + 10ms =15ms typical

Typical total delays at Vo2 = Ton delays from EN2 + Ton rise delays = 10ms + 5ms =15ms typical

T-off delay

During the shut-down of the converter, the controller doesn't need to wait for the preparation of the reference ramp. The propagation delay from Enable signal to PWM off is very small, and Vout can almost follow the T-off delay setting to turn off the output. However, note that the controller is not able to ensure whether it reads EN1 status or EN2 status first, and therefore there if the unit is used in 2 output configuration, there will be a delay in Enable OFF between two channel outputs. The delay between the two channels is 0.1ms typical.

Configuration Setting (CFG)

The Configuration pin (CFG) sets several module configuration settings allowing the module to be used in applications without the need for loading configuration files. The settings are shown in Table 9. This must be done in order for the 2 modules to be recognized as part of a current sharing group.

Table 9. Configuration Setting Reference:

RCFG(Kohm)	CIRCUIT
90.9	4-PH Master
100	4-PH Slave
LOW	2-Phase
OPEN	2 Output

Charge Mode Control (ASCR) Setting(ASCRCFG)

The module's Charge Mode response can be optimized by adjusting the ASCR Gain and Residual settings by using the ASCR_CONFIG PMBus™ command or external resister between ASCR and GND. The resister setting is followed Table 10.

Table 10. Charge Mode Control Setting Reference:

ASCRCFG(Kohm)	GAIN Phase2	GAIN Phase1
10	200	200
17.8	400	400
31.6	600	600
56.2	800	800
110	100	100
121	300	300
133	500	500
147	700	700
LOW	300	300
OPEN	500	500
HIGH	700	700

Note: ASCR gain must be set to same value of each phase at 2,4,6,8 phase application.

Multi Phase (TBD)

Extra commands are required for 4, 6 or 8 phase application. Table 11 and Table 12 is an example for 8 phase commands setting. Artesyn qualified Vin = 12V for 8 phase application only.

Table 11, Command setting for 8 phase

<table>
<tr><th></th><th>Command Name</th><th>Master module</th><th>Slave module 1</th><th>Slave module 2</th><th>Slave module 3</th></tr>
<tr><td>Global</td><td>USER_GLOBAL_CONFIG</td><td>0x1102</td><td>0x1104</td><td>0x1104</td><td>0x1104</td></tr>
<tr><td rowspan="4">Page 0</td><td>DDC_CONFIG</td><td>0x0007</td><td>0x2007</td><td>0x4007</td><td>0x6007</td></tr>
<tr><td>DDC_GROUP</td><td>0x00202000</td><td>0x00202000</td><td>0x00202000</td><td>0x00202000</td></tr>
<tr><td>VOUT_DROOP</td><td colspan="4" rowspan="2">Table 12</td></tr>
<tr><td>MULTI_PHASE_RAMP_GAIN</td></tr>
<tr><td rowspan="4">Page 1</td><td>DDC_CONFIG</td><td>0x8007</td><td>0xA007</td><td>0xC007</td><td>0xE007</td></tr>
<tr><td>DDC_GROUP</td><td>0x00202000</td><td>0x00202000</td><td>0x00202000</td><td>0x00202000</td></tr>
<tr><td>VOUT_DROOP</td><td colspan="4" rowspan="2">Table 12</td></tr>
<tr><td>MULTI_PHASE_RAMP_GAIN</td></tr>
</table>

Table 12, Recommended Vout_Droop and MULTI_PHASE_RAMP_GAIN setting for 8 Phase

Vout (V)	Vout Droop	MULTI_PHASE_RAMP_GAIN
0.6	0.13 (0xA214)	3 (0x03)
1	0.13 (0xA214)	3 (0x03)
1.8	0.13 (0xA214)	7(0x07)
2.5	0.13 (0xA214)	7(0x07)
3.3	0.1 (0x9B33)	15(0x0F)
5	0.2 (0xA333)	15(0x0F)

Multi Phase – Current derating at low temperature (TBD)

For 4, 6 or 8 Phase, current derating is required at low temperature. Refer to Table 13 .

Table 13 , 4, 6 or 8 Phase current derating table at low temperature

	-20 °C	**-40 °C**
Vout (V)	**Max Iout (per phase)**	**Max Iout (per phase)**
0.6	25A	23A
1	25A	25A
1.8	22A	20A
2.5	17A	17A
3.3	14A	14A

Surface Mount Information

Pick and Place

The LGA50D is designed with certain features to ensure it is compatible with standard pick and place equipment.
The low mass of typically 9 grams is within the capability of standard pick and place equipment. The choice of nozzle size and style and placement speed may need to be optimized.

The inductor has a flat area of 263.8mm2 (0.409in^2) that can be used as a pick-up area.

PC Board Assembly Side

LGA50D module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Moisture Sensitivity Level (MSL)

This module is classified as MSL level 3

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of <= 30ºC and 60% relative humidity varies according to the MSL rating (See J-STD-033). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: <40ºC, <90% relative humidity.

Post Soldering Cleaning

Post solder cleaning is not recommended because it may affect the reliability of module.

Pb-free Reflow Profile

This module will comply with IPC/JEDEC J-STD-020 (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. The Standard provides reflow profile based on the volume and thickness of the module. The suggested Pb-free solder paste is Sn/Ag/Cu (SAC305). The recommended reflow temperature profile using SAC305 solder is shown below.

Tin-Pb Reflow Profile

The power modules are lead free modules and can be soldered either in a lead-free solder process or in a conventional Tin/Lead (Sn/Pb) process. It is recommended that the customer review datasheets in order to customize the solder reflow profile for each load board assembly. The following instructions must be observed when soldering these units. Failure to observe there instructions may result in the failure of or cause damage to the modules, and can adversely affect long-term reliability.

In a conventional Tin/Lead (Sn/Pb) solder process, peak reflow temperatures are limited to less than 235ºC. Typically, the eutectic solder melts at 183ºC, wets the land, and subsequently wicks the device connection. Sufficient time must be allowed to fuse the plating on the connection ensure a reliable solder joint. There are several types of SMTreflow technologies currently used in the industry. These surface mount power modules can be reliably soldered using natural forced convection, IR (radiant infrared), or a combination of convection/IR. For reliable soldering the solder reflow profile should be established by accurately measuring the modules block pin temperatures.

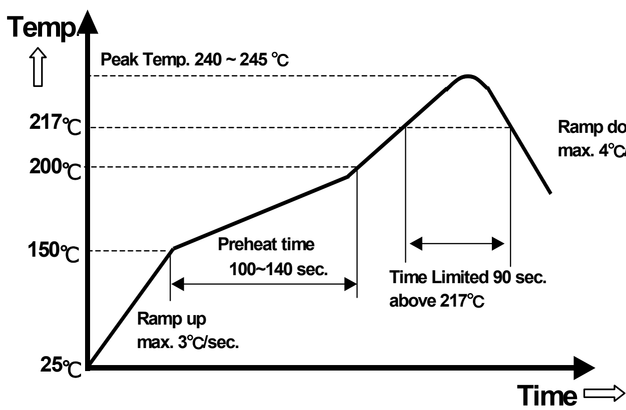


Figure 65 Recommended reflow profile using SAC305 solder paste

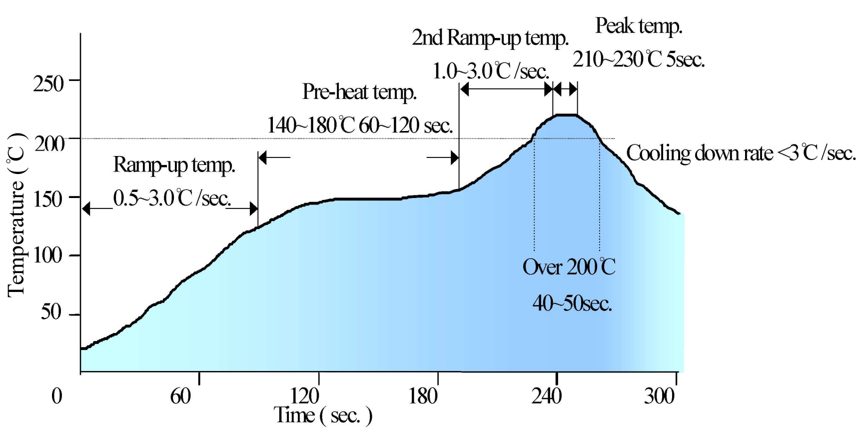
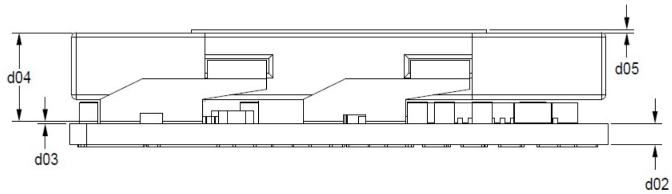


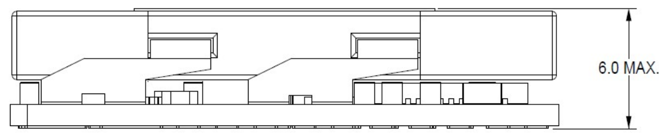
Figure 66 Recommended reflow profile

Note: 1. The stencil thickness for soldering module to load board is recommended as 5mil.
2. Recommended soldering Nitrogen process.

Module Dimensions after Mounting

The following data shows the analysis height-tolerance that is expected for the LGA50D-01DADJLPJ and LGA50D-01DADJLP1J module after it has been mounted to the host application PCB.





Ref	Description	Design Data Feature Type	Feature Dimension	
D02	PCB thickness	Other	1.00	+0.10
				-0.10
D03	Solder paste per max value	Other	0.0237	+0.0193
				-0.0193
D04	Inductor per max.height	Catalogue Size	4.60	+0.00
				-0.00
D05	Label thickness	Catalogue Size	0.065	+0.004
				-0.004

Arithmetic Worst Case (AWC) Analysis

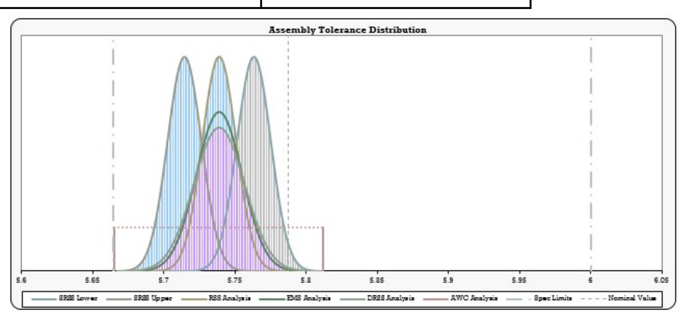
Use for safety critical dimensions

Arithmetic Worst Case Analysis assumes all tolerances are at their worst extreme and that all out of specification parts have been removed through inspection.

Note: the nominal dimension is in the positive sense.

Nominal Dimension		Expected Value		Limit Values	Spec Parts All pass
5.7887	+0.0233	5.7387	+0.0733	5.812 5.6654	Yes
	-0.1233		-0.0733		

	Extremes of Fit wrt	
	Minimum	Maximum
Upper Spec Limit	+0.3346	+0.188
Lower Spec Limit	+0.001	-0.1476



Height :

Nominal = 5.7877 + 0.06 (solder bump thk.)= 5.8477mm

Maximum = 5.812 + 0.06 (solder bump thk)= 5.872mm

Minimum = 5.6654 + 0.06 (solder bump thk)= 5.7254mm

Record of Revision and Changes

Issue	Date	Description	Originators
1.0	01.07.2018	First Issue	K. Wang
1.1	03.06.2019	Update the type on first page	K. Wang