LGA C Series

15-100 Watts
Non Isolated DCDC Converter

Total Power:	15-100 W
Input Voltage:	3-14 Vdc
# of Outputs:	Single

Special Features

- 3, 6, 10 and 20 A output current rating
- Wide input voltage range; up to 14 V
- Adjustable output voltage; 0.59-5.1 V
- Excellent transient response
- High efficiency
- Output margining
- Power enable
- Minimal airflow requirement
- Termination voltage capability
- Ultra compact profile and footprint
- Remote sense
- RoHS compliant

Safety

Designed to meet EN60950

International Standards for Solderability: J-STD-002B IEC-60068-2-58

RoHS

Product Descriptions

The LGA C Series is a high density, non-isolated board-mounted DC-DC converter for space sensitive applications. This Embedded Power Device (EPD) has a wide input range up to14 V and offers a 0.59-5.1 V adjustable output with 3, 6, 10 and 20 A capability without derating. This EPD offers a complete feature set of enable, remote sense, and power good inclusive of a wide adjustable output range.

Applications

ASIC, Memory, FPGAs, Telecom and Networking Equipment, Servers, Industrial Equipment, POL Regulation.

ARTESYN EMBEDDED TECHNOLOGIES

Model Numbers

Model Number	Input Voltage	Output Voltage	Minimum Load	Maximum Load
LGA03C-00SADJJ	3-14Vdc	0.59-5.1Vdc	0A	3A
LGA06C-00SADJJ	3-14Vdc	0.59-5.1Vdc	0A	6A
LGA10C-00SADJJ	3-14Vdc	0.59-5.1Vdc	0A	10A
LGA20C-01SADJJ	4.5-14Vdc	0.59-5.1Vdc	0A	20A

Ordering information

LGA	03	C	-	00	SADJ	X	J
①	②	③		④	⑤	⑥	⑦

①	Model series	LGA: Land Grid Array
②	Rated Output Current	03: 3A 06: 6A 10: 10A 20: 20A
③	Performance	C: Cost optimized
④	Input Voltage Range	00: 3 - 14Vdc 01: 4.5 - 14Vdc
⑤	Type of Outputs	SADJ: Single Adjustable Output
⑥	Options	X: Various Options (see Sales Rep)
⑦	RoHS	J: Pb free (RoHS 6/6 compliant)

Options

None

Electrical Specifications

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings:

Parameter	Model	Symbol	Min	Nom	Max	Unit
Input Voltage (DC continuous operation)	All models	V_{IN}	0	-	14	Vdc
Maximum Output Power	LGA03C LGA06C LGA10C LGA20C	$P_{O,max}$	- - - -	- - - -	15 30 50 100	W
Enable Voltage	All models		0	-	5	Vdc
Operating Ambient Temperature[1]	All models	T_A	-40	-	+85	^OC
Storage Temperature	All models	T_{STG}	-40	-	+125	^OC
Case Temperature	All models	T_C	-	-	+100	^OC

Note 1 - The LGA C Series module has an operating temperature range of -40 ^OC to 85 ^OC with suitable derating. See detailed derating curves.

Input Specifications

Table 2. Input Specifications:

Parameter		Conditions	Symbol	Min	Nom	Max	Unit
Operating Input Voltage, DC	LGA03C LGA06C LGA10C LGA20C	All	V_{IN}	3 3 3 4.5	- - - -	14 14 14 14	Vdc
Maximum Input Current	LGA03C LGA06C LGA10C LGA20C	All	$I_{IN,max}$	- - - -	- - - -	3 6 10 20	A
Standby Input Current	LGA03C LGA06C LGA10C LGA20C	V_{IN}=12V, V_O=Off	$I_{IN,standby}$	- - - -	14 14 14 13	- - - -	mA
No Load Input Current	LGA03C LGA06C LGA10C LGA20C	V_{IN}=12V, V_O=2.5V, I_O=0A	$I_{IN,no-load}$	- - - -	55 94 100 87	- - - -	mA
Efficiency	LGA03C (I_O=3A)	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	η	- - -	79.1 86.4 91.8	- - -	%
	LGA06C (I_O=6A)	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	η	- - -	80.1 86.5 92.1	- - -	%
	LGA10C (I_O=10A)	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	η	- - -	76.6 85.9 91.7	- - -	%
	LGA20C (I_O=20A)	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	η	- - -	77.3 86.6 91.2	- - -	%
Input Capacitance (Internal)				-	10	-	uF
Input Capacitor (External)		Required for input ripple current		-	1	-	uF

Output Specifications

Table 3. Output Specifications:

Parameter		Conditions	Symbol	Min	Nom	Max	Unit
Output Voltage		All	V_O	0.59	-	5.1	Vdc
Output Current	LGA03C LGA06C LGA10C LGA20C	All	I_O	0 0 0 0	- - - -	3 6 10 20	A A A A
Output Set-point Accuracy		0.1% trim resistors	$\%V_O$	-1	-	+1	%
Output Line Regulation		All	$\%V_O$	-0.2	-	+0.2	%
Output Load Regulation		All	$\%V_O$	-0.5	-	+0.5	%
Turn On Delay		From V_{IN} or Enable	$T_{turn-on}$	-	2	3	mS
Output Rise Time		From 10% to 90%V_O	T_{rise}	-	1.5	-	mS
Output Ripple and Noise (with 10uF output cap)	LGA03C	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	V_O	- - -	15 20 30	- - -	mV_{PK-PK}
	LGA06C	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	V_O	- - -	20 35 50	- - -	mV_{PK-PK}
	LGA10C	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	V_O	- - -	30 40 45	- - -	mV_{PK-PK}
	LGA20C	V_{IN}=5V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	V_O	- - -	25 45 70	- - -	mV_{PK-PK}
Enable Specifications	Signal Low Voltage	Unit Off		0	-	0.4	V
	Signal Low Current	V_{IN}=12V		0	400	-	uA
	Signal High Voltage	Unit On		15	-	-	V
	Signal High Current			-	1	-	uA
Flammability		All	UL94V-0				
Moisture Sensitivity Level (MSL)		All	3				
Material Type		All	FR4 PCB				
Solderability			J-STD-002B IEC-60068-2-58				

Output Specifications

Table 3. Output Specifications, con't:

Parameter		Conditions	Symbol	Min	Nom	Max	Unit
Output Capacitance (Internal)		All	C_O	-	20	-	uF
Output Startup Capacitance (External)	LGA03C	V_{IN}=12V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	C_O	10 10 10	- - -	3300 1100 450	uF
	LGA06C	V_{IN}=12V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	C_O	10 10 10	- - -	7500 1500 750	uF
	LGA10C	V_{IN}=12V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	C_O	10 10 10	- - -	7500 2400 1200	uF
	LGA20C	V_{IN}=12V, V_O=0.9V V_{IN}=12V, V_O=2.5V V_{IN}=12V, V_O=5V	C_O	50 50 50	- - -	7500 2400 500	uF
LGA03C Dynamic Load Response[1]	Peak Deviation	V_O=0.9V 1.5-3A step load	$\pm V_O$	-	85	-	mV
	Setting Time		T_s	-	8	-	uS
	Peak Deviation	V_O=2.5V 1.5-3A step load	$\pm V_O$	-	95	-	mV
	Setting Time		T_s	-	15	-	uS
LGA06C Dynamic Load Response[1]	Peak Deviation	V_O=0.9V 3-6A step load	$\pm V_O$	-	125	-	mV
	Setting Time		T_s	-	8	-	uS
	Peak Deviation	V_O=2.5V 3-6A step load	$\pm V_O$	-	175	-	mV
	Setting Time		T_s	-	8	-	uS
LGA10C Dynamic Load Response[1]	Peak Deviation	V_O=0.9V 5-10A step load	$\pm V_O$	-	90	-	mV
	Setting Time		T_s	-	8	-	uS
	Peak Deviation	V_O=2.5V 5-10A step load	$\pm V_O$	-	135	-	mV
	Setting Time		T_s	-	8	-	uS
LGA20C Dynamic Load Response[1]	Peak Deviation	V_O=0.9V 10-20A step load	$\pm V_O$	-	95	-	mV
	Setting Time		T_s	-	12	-	uS
	Peak Deviation	V_O=2.5V 10-20A step load	$\pm V_O$	-	175	-	mV
	Setting Time		T_s	-	20	-	uS

Note 1 - For all the dynamic load response test, V_{IN}=12V, slew rate is 5A/uS. Output capacitance is 10uF for LGA03C, LGA06C and LGA10C, 50uF for LGA20C.

Output Specifications

Table 3. Output Specifications, con't:

Parameter		Conditions	Symbol	Min	Nom	Max	Unit
Over Current Protection	LGA03C	Hiccup Mode	I_O	-	6	-	A
	LGA06C		I_O	-	11	-	A
	LGA10C		I_O	-	20	-	A
	LGA20C		I_O	-	27	-	A
Switching Frequency	LGA03C	All	f_{SW}	-	1000	-	kHz
	LGA06C		f_{SW}	-	1000	-	kHz
	LGA10C		f_{SW}	-	1000	-	kHz
	LGA20C		f_{SW}	-	800	-	kHz
Junction to Case Thermal Resistance	LGA03C	All		-	3	-	$^OC/W$
	LGA06C			-	3	-	$^OC/W$
	LGA10C			-	9	-	$^OC/W$
	LGA20C			-	2	-	$^OC/W$
MTBF		Telcordia SR-332 $T_A=40^OC$ Full Load		-	20	-	MHours
Weight		All		-	0.1	-	oz

LGA03C-00SADJJ Performance Curves

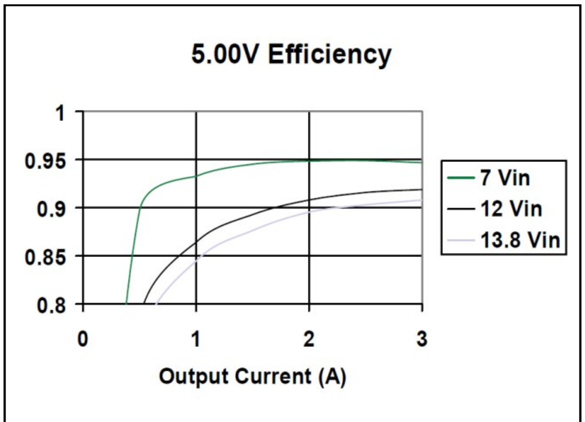


Figure 1: LGA03C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 3A, Vo= 5V

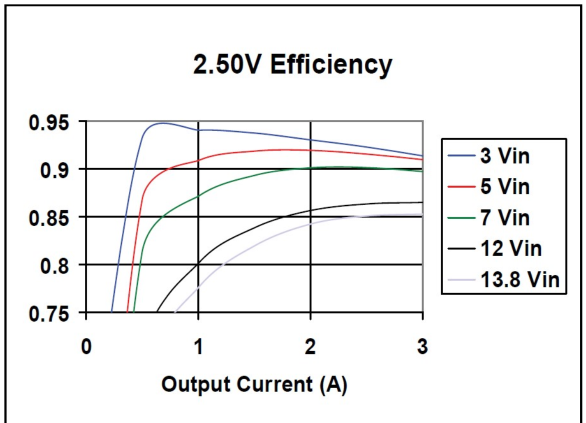


Figure 2: LGA03C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 3A, Vo= 2.5V

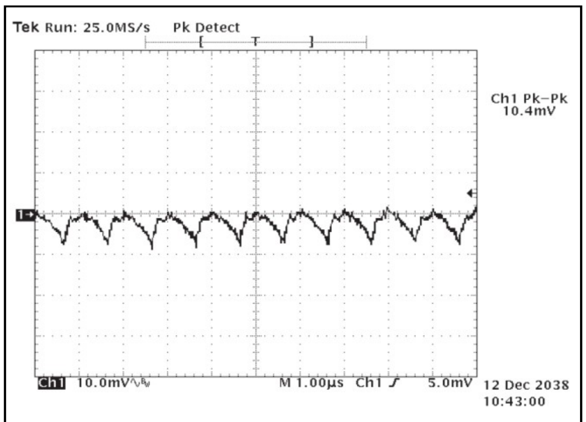


Figure 3: LGA03C-00SADJJ Ripple and Noise Measurement

Ch 1: Vo

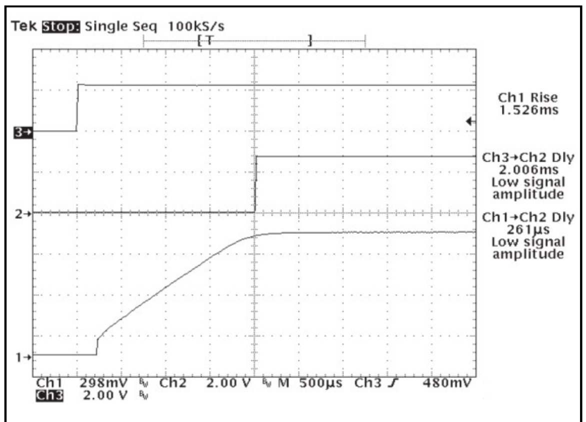


Figure 4: LGA03C-00SADJJ Output Voltage Startup Characteristic by Remote

Ch1: Vo Ch2: PGOOD Ch3: Remote On/Off

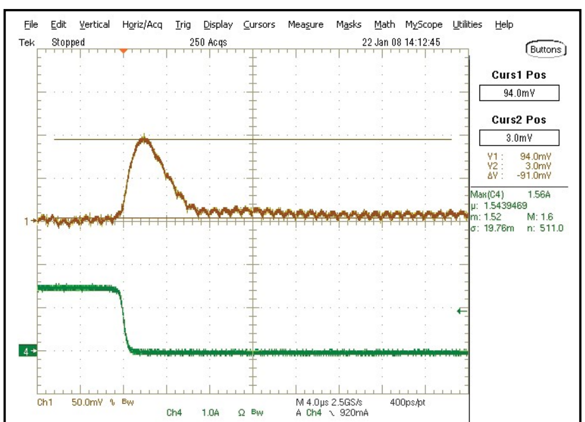


Figure 5: LGA03C-00SADJJ Transient Response
Load: Io = 100% to 50% load change
Ch 1: Vo Ch4: Io (1A/div)

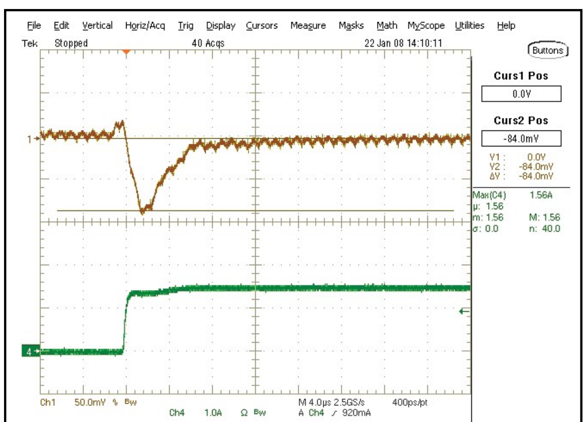


Figure 6: LGA03C-00SADJJ Transient Response
Load: Io = 50% to 100% load change
Ch 1: Vo Ch4: Io (1A/div)

LGA03C-00SADJJ Performance Curves

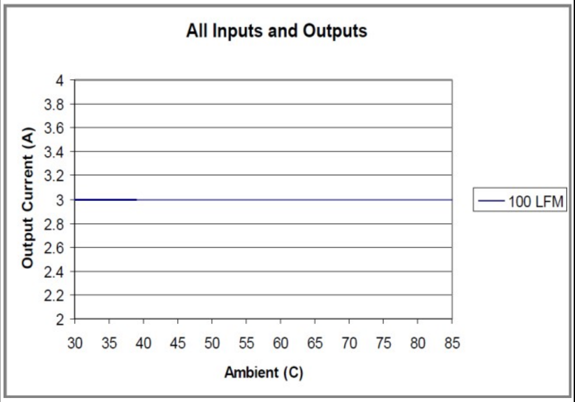


Figure 7: LGA03C-00SADJJ Thermal Derating Curve for All Inputs and Outputs

LGA06C-00SADJJ Performance Curves

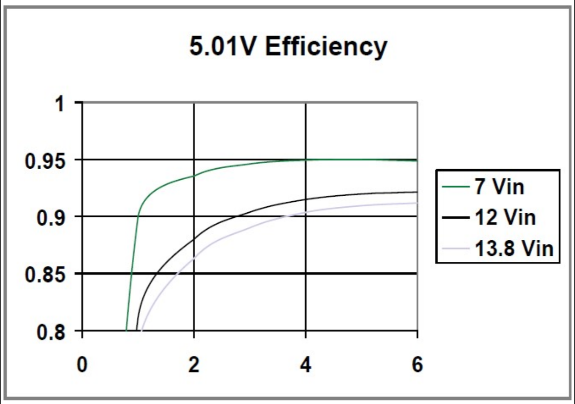


Figure 8: LGA06C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 6A, Vo= 5.01V

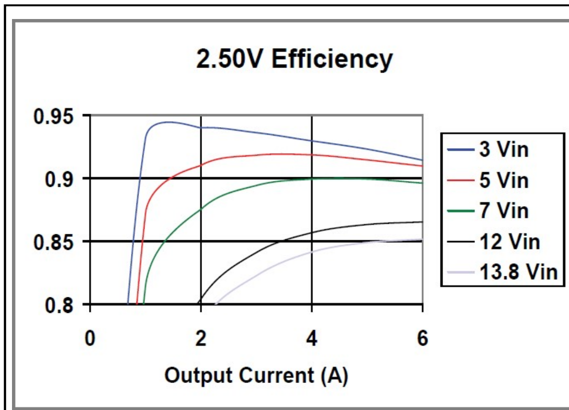


Figure 9: LGA06C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 6A, Vo= 2.5V

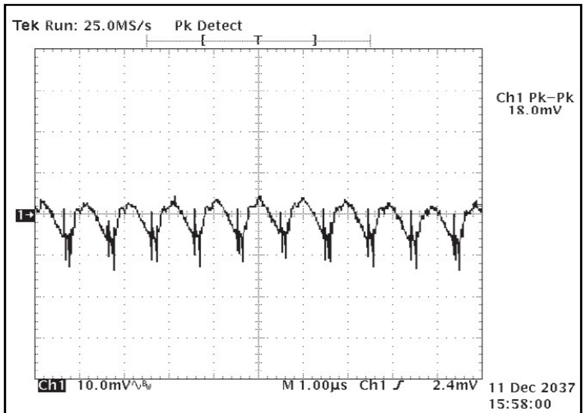


Figure 10: LGA06C-00SADJJ Ripple and Noise Measurement

Ch 1: Vo

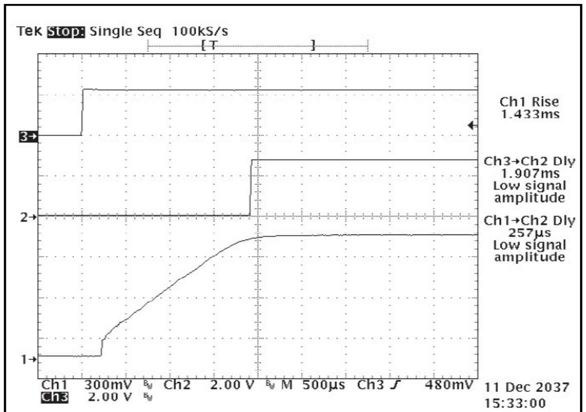


Figure 11: LGA06C-00SADJJ Output Voltage Startup Characteristic by Remote

Ch1: Vo Ch2: PGOOD Ch3: Remote On/Off

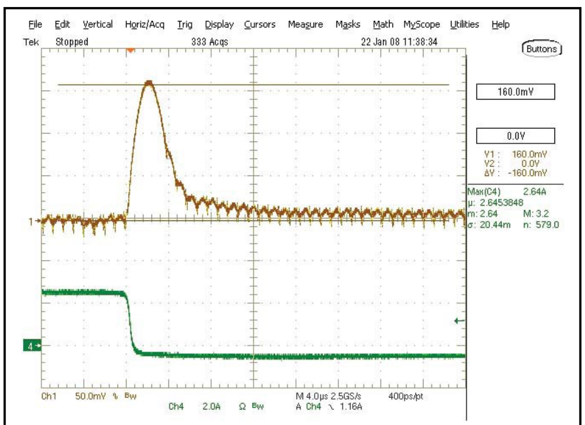


Figure 12: LGA06C-00SADJJ Transient Response
Load: Io = 100% to 50% load change
Ch 1: Vo Ch4: Io (2A/div)

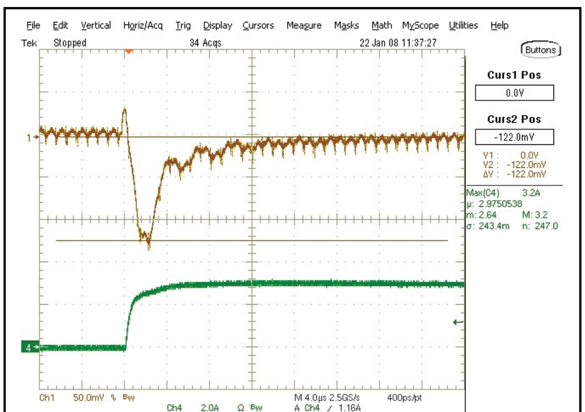


Figure 13: LGA06C-00SADJJ Transient Response
Load: Io = 50% to 100% load change
Ch 1: Vo Ch4: Io (2A/div)

LGA06C-00SADJJ Performance Curves

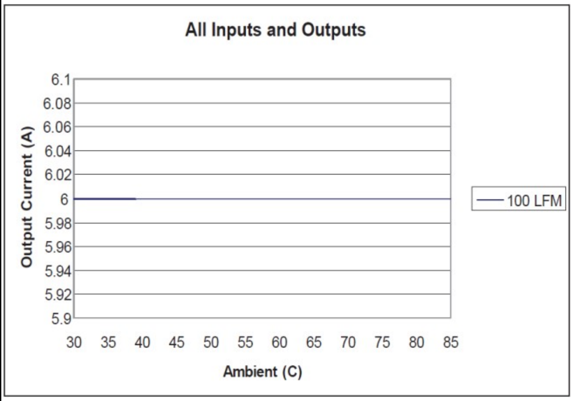


Figure 14: LGA06C-00SADJJ Thermal Derating Curve for All Inputs and Outputs

LGA10C-00SADJJ Performance Curves

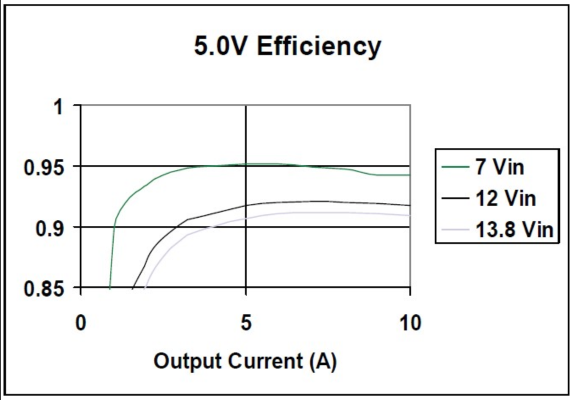


Figure 15: LGA10C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 10A, Vo= 5V

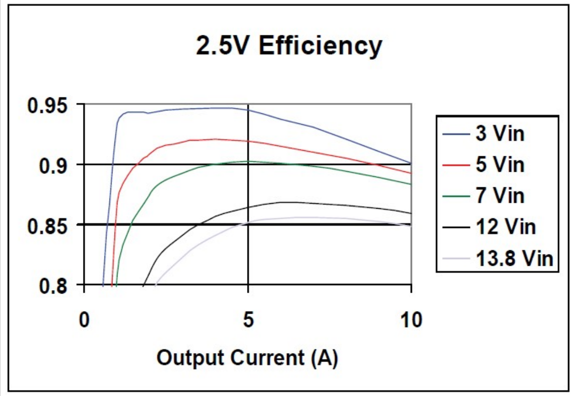


Figure 16: LGA10C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 10A, Vo= 2.5V

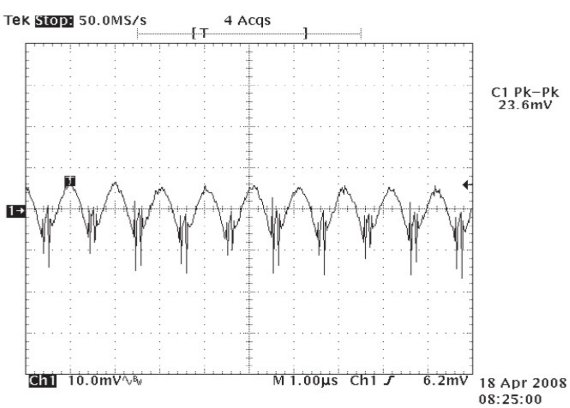


Figure 17: LGA10C-00SADJJ Ripple and Noise Measurement

Ch 1: Vo

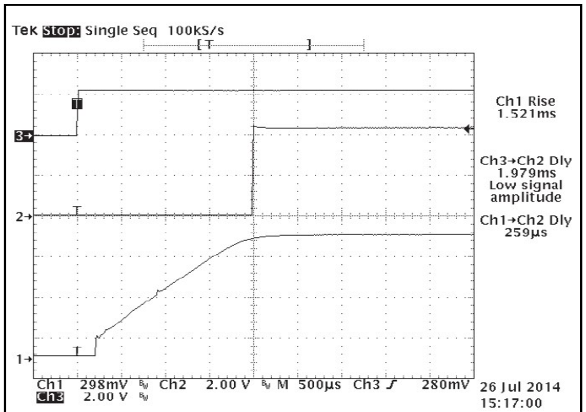


Figure 18: LGA10C-00SADJJ Output Voltage Startup Characteristic by Remote

Ch1: Vo Ch2: PGOOD Ch3: Remote On/Off

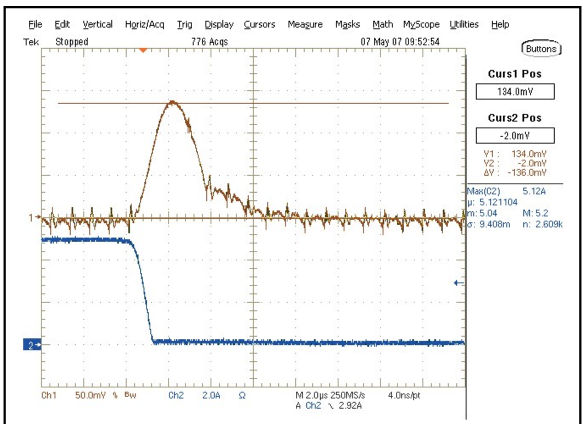


Figure 19: LGA10C-00SADJJ Transient Response
Load: Io = 100% to 50% load change
Ch 1: Vo Ch4: Io (2A/div)

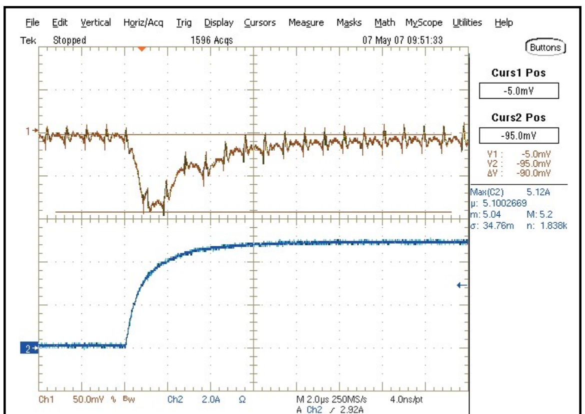


Figure 20: LGA10C-00SADJJ Transient Response
Load: Io = 50% to 100% load change
Ch 1: Vo Ch4: Io (2A/div)

LGA10C-00SADJJ Performance Curves

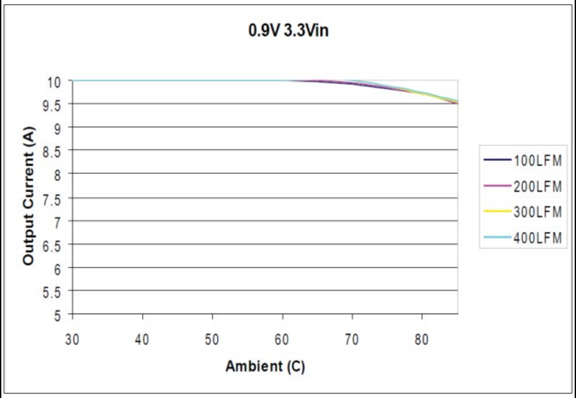


Figure 21: LGA10C-00SADJJ Thermal Derating Curve

Vin = 3.3Vdc, Load: Io = 0 to 10A, Vo= 0.9V

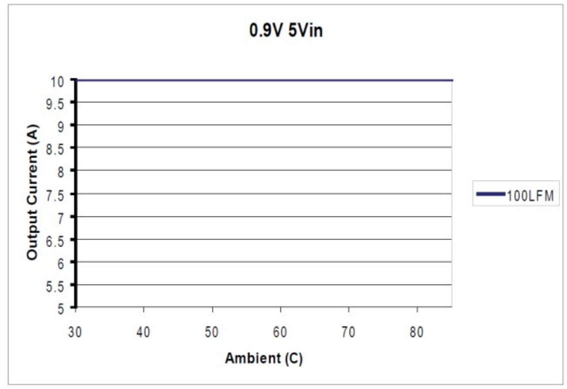


Figure 22: LGA10C-00SADJJ Thermal Derating Curve

Vin = 5Vdc, Load: Io = 0 to 10A, Vo= 0.9V

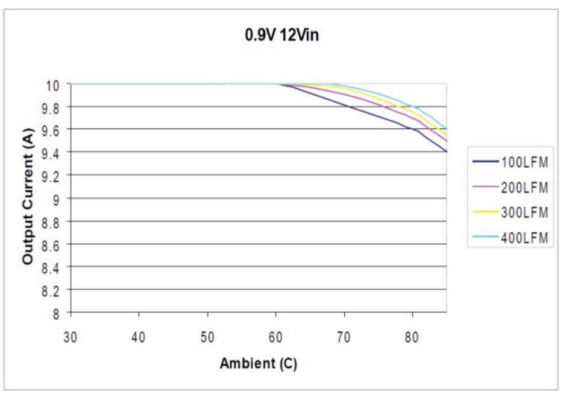


Figure 23: LGA10C-00SADJJ Thermal Derating Curve

Vin = 12Vdc, Load: Io = 0 to 10A, Vo= 0.9V

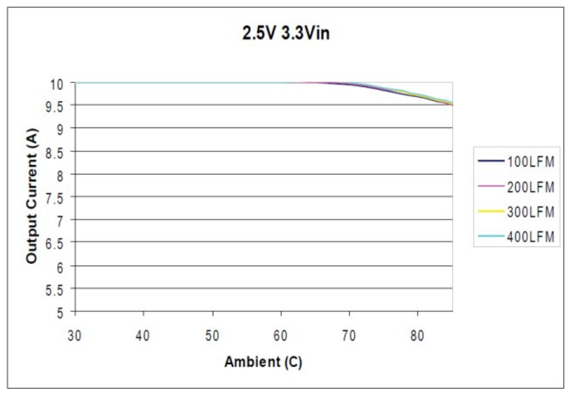


Figure 24: LGA10C-00SADJJ Thermal Derating Curve

Vin = 3.3Vdc, Load: Io = 0 to 10A, Vo= 2.5V

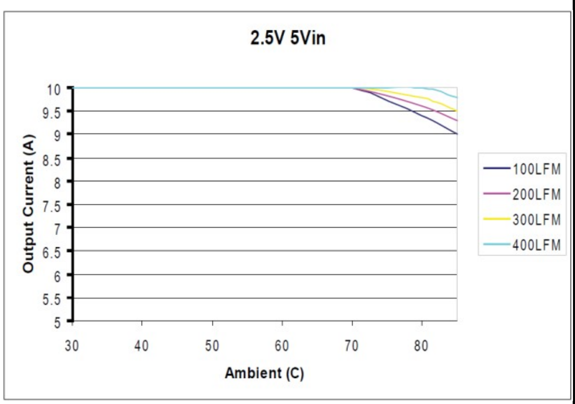


Figure 25: LGA10C-00SADJJ Thermal Derating Curve

Vin = 5Vdc, Load: Io = 0 to 10A, Vo= 2.5V

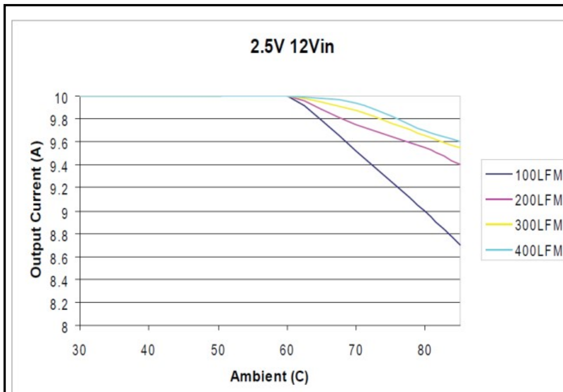


Figure 26: LGA10C-00SADJJ Thermal Derating Curve

Vin = 12Vdc, Load: Io = 0 to 10A, Vo= 2.5V

LGA10C-00SADJJ Performance Curves

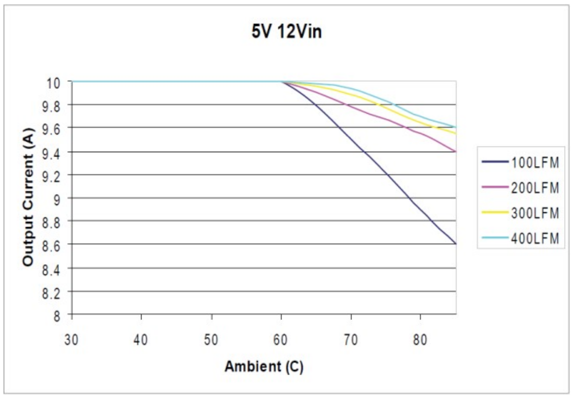


Figure 27: LGA10C-00SADJJ Thermal Derating Curve

Vin = 12Vdc, Load: Io = 0 to 10A, Vo= 5V

LGA20C-00SADJJ Performance Curves

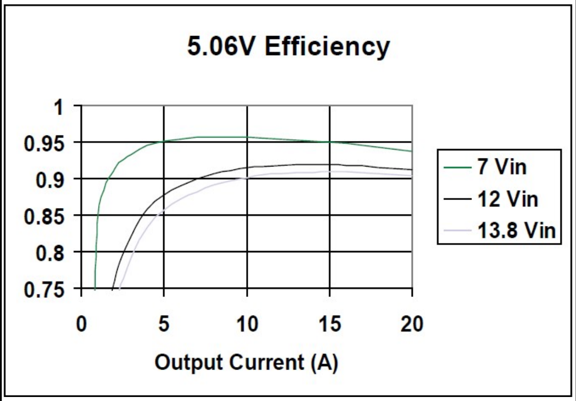


Figure 28: LGA20C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 20A, Vo= 5.06V

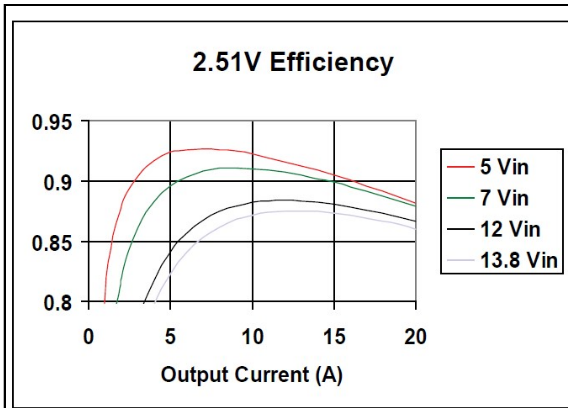


Figure 29: LGA20C-00SADJJ Efficiency Curve

Loading: Io = 10% increment to 20A, Vo= 2.51V

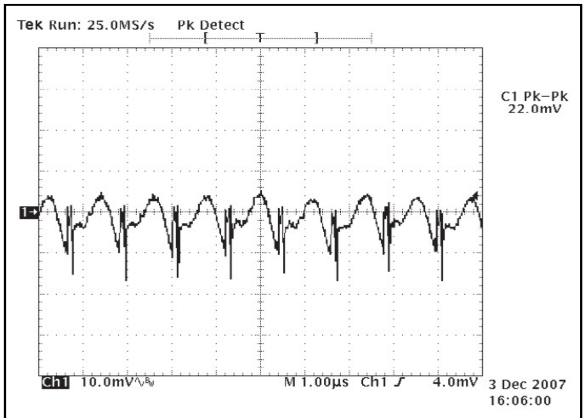


Figure 30: LGA20C-00SADJJ Ripple and Noise Measurement

Ch 1: Vo

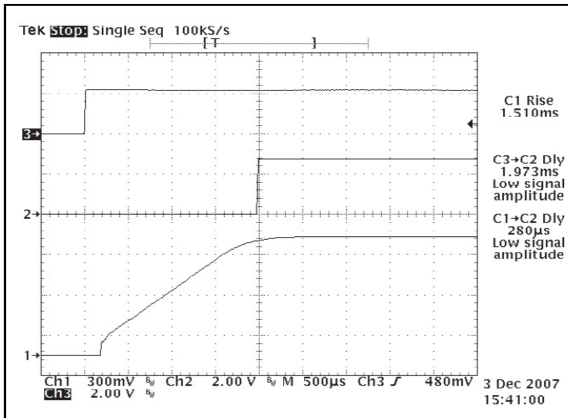


Figure 31: LGA20C-00SADJJ Output Voltage Startup Characteristic by Remote

Ch1: Vo Ch2: PGOOD Ch3: Remote On/Off

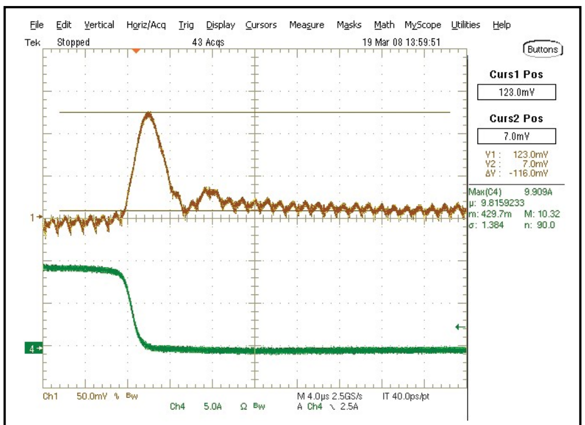


Figure 32: LGA20C-00SADJJ Transient Response
Load: Io = 100% to 50% load change
Ch 1: Vo Ch4: Io (5A/div)

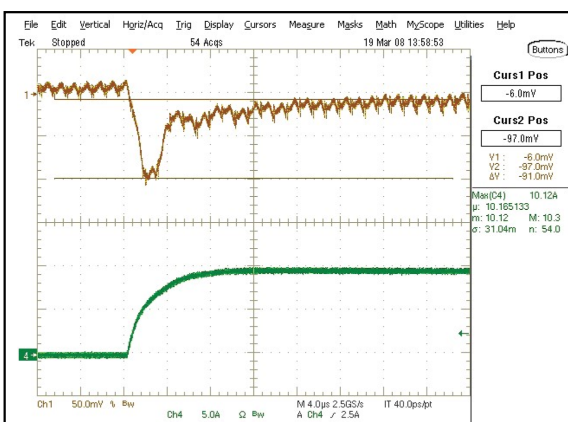


Figure 33: LGA20C-00SADJJ Transient Response
Load: Io = 50% to 100% load change
Ch 1: Vo Ch4: Io (5A/div)

LGA20C-00SADJJ Performance Curves

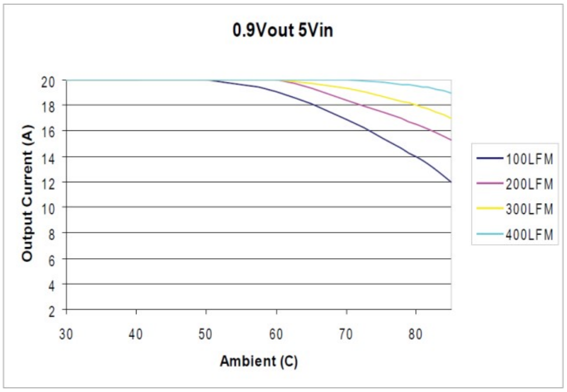


Figure 34: LGA20C-00SADJJ Thermal Derating Curve

Vin = 5Vdc, Load: Io = 0 to 20A, Vo= 0.9V

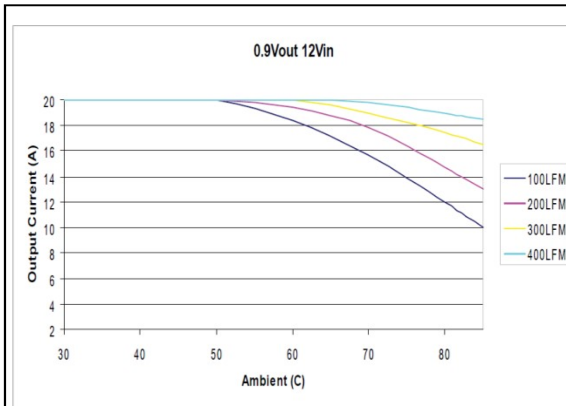


Figure 35: LGA20C-00SADJJ Thermal Derating Curve

Vin = 12Vdc, Load: Io = 0 to 20A, Vo= 0.9V

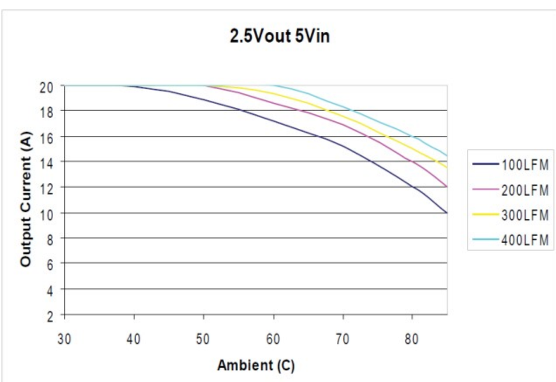


Figure 36: LGA20C-00SADJJ Thermal Derating Curve

Vin = 5Vdc, Load: Io = 0 to 20A, Vo= 2.5V

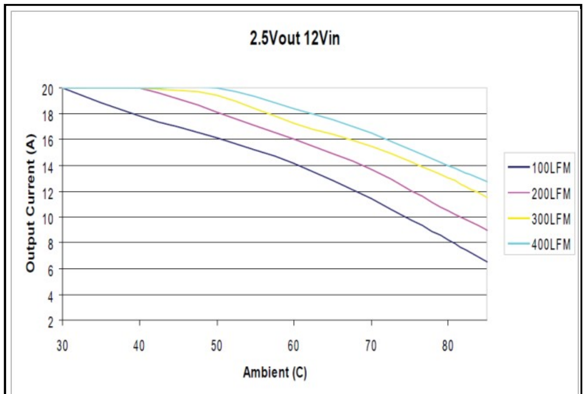


Figure 37: LGA20C-00SADJJ Thermal Derating Curve

Vin = 12Vdc, Load: Io = 0 to 20A, Vo= 2.5V

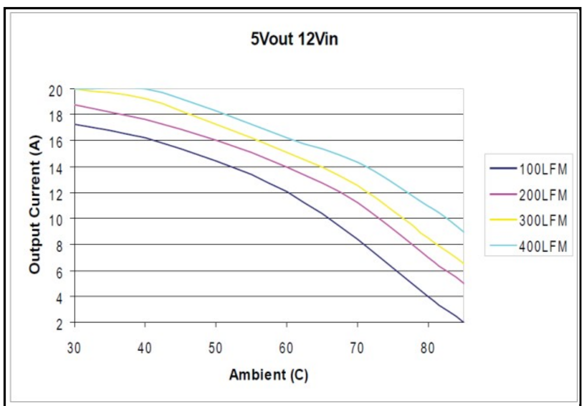


Figure 38: LGA20C-00SADJJ Thermal Derating Curve

Vin = 12Vdc, Load: Io = 0 to 20A, Vo= 5V

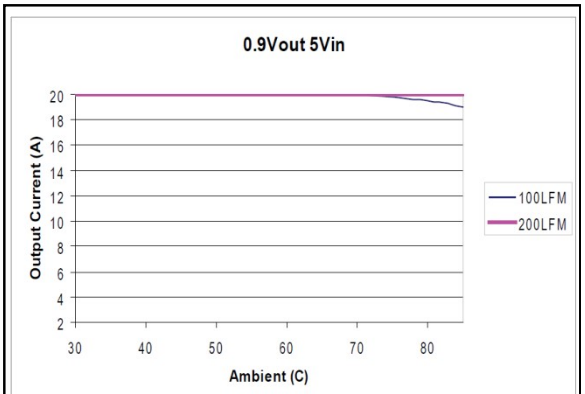


Figure 39: LGA20C-00SADJJ Thermal Derating Curve with 0.5" Heatsink

Vin = 5Vdc, Load: Io = 0 to 20A, Vo= 0.9V

LGA20C-00SADJJ Performance Curves

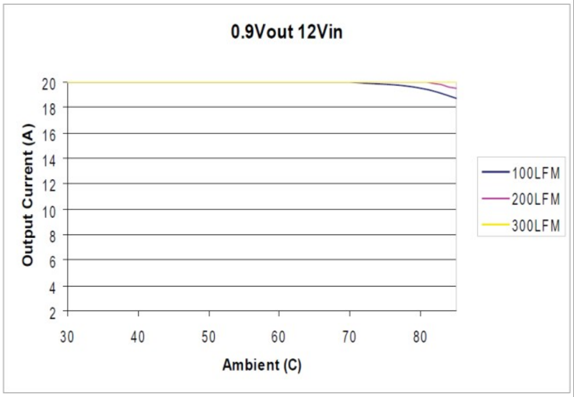


Figure 40: LGA20C-00SADJJ Thermal Derating Curve with 0.5" Heatsink

Vin = 12Vdc, Load: Io = 0 to 20A, Vo= 0.9V

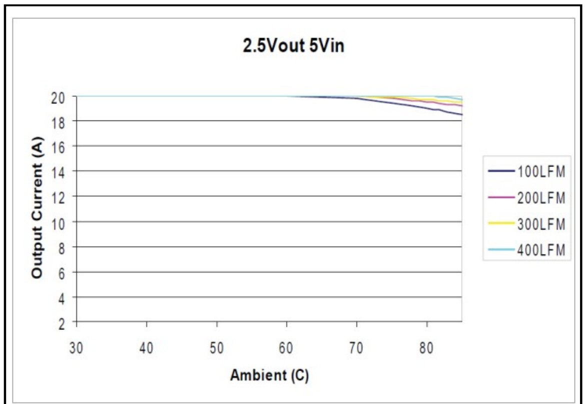


Figure 41: LGA20C-00SADJJ Thermal Derating Curve with 0.5" Heatsink

Vin = 5Vdc, Load: Io = 0 to 10A, Vo= 2.5V

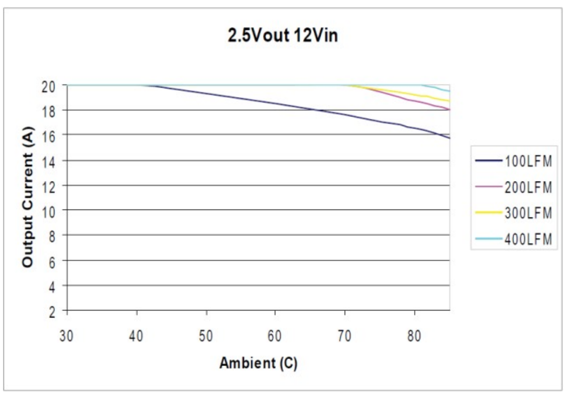


Figure 42: LGA20C-00SADJJ Thermal Derating Curve with 0.5" Heatsink

Vin = 12Vdc, Load: Io = 0 to 20A, Vo= 2.5V

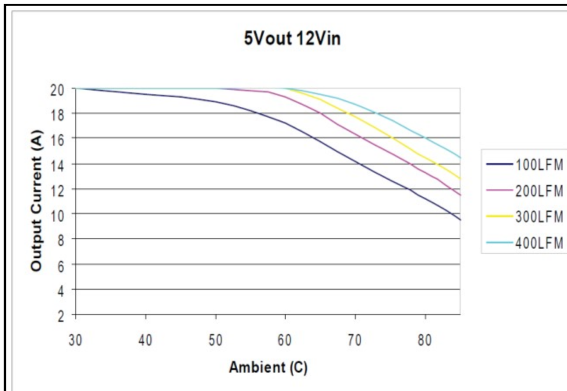


Figure 43: LGA20C-00SADJJ Thermal Derating Curve with 0.5" Heatsink

Vin = 12Vdc, Load: Io = 0 to 20A, Vo= 5V

Protection Function Specification

Current Limit and Short-Circuit Protection

The LGA C models have a built-in non-latching current limit function and full continuous short-circuit protection. The module monitors current through the top and bottom FET. When an overcurrent condition occurs, the module goes into hiccup mode, where it attempts to power up periodically to determine if the problem persists.

The output current level is sensed through the voltage drop across the top and bottom FETs during their on time. This type of sensing is affected by temperature due to the change in Rdson. At higher temperatures, the Rdson increases, which lowers the overcurrent point.

Note that the module specifications are not guaranteed when the unit is operated in an overcurrent condition.

Undervoltage Lockout (UVLO)

The LGA C models have built-in undervoltage lockout to ensure reliable output power. The lockout prevents the unit from operating when the input voltage is too low.

The default undervoltage lockout is set as follows:

LGA 3/6/10C: 2.9 V

LGA20C: 4.3 V

The UVLO for the LGA03/06/10C can be adjusted with the following equation:

$$R_{uvlo} = \frac{14.8 \times 6.81}{6.81 \times V_{turn\_on} - 18.16} (K\Omega)$$

The UVLO for the LGA20C can be adjusted with the following equation:

$$R_{uvlo} = \frac{30.1 \times 4.22}{8.577 \times V_{turn\_on} - 34.32} (K\Omega)$$

Mechanical Specifications

Mechanical Drawing

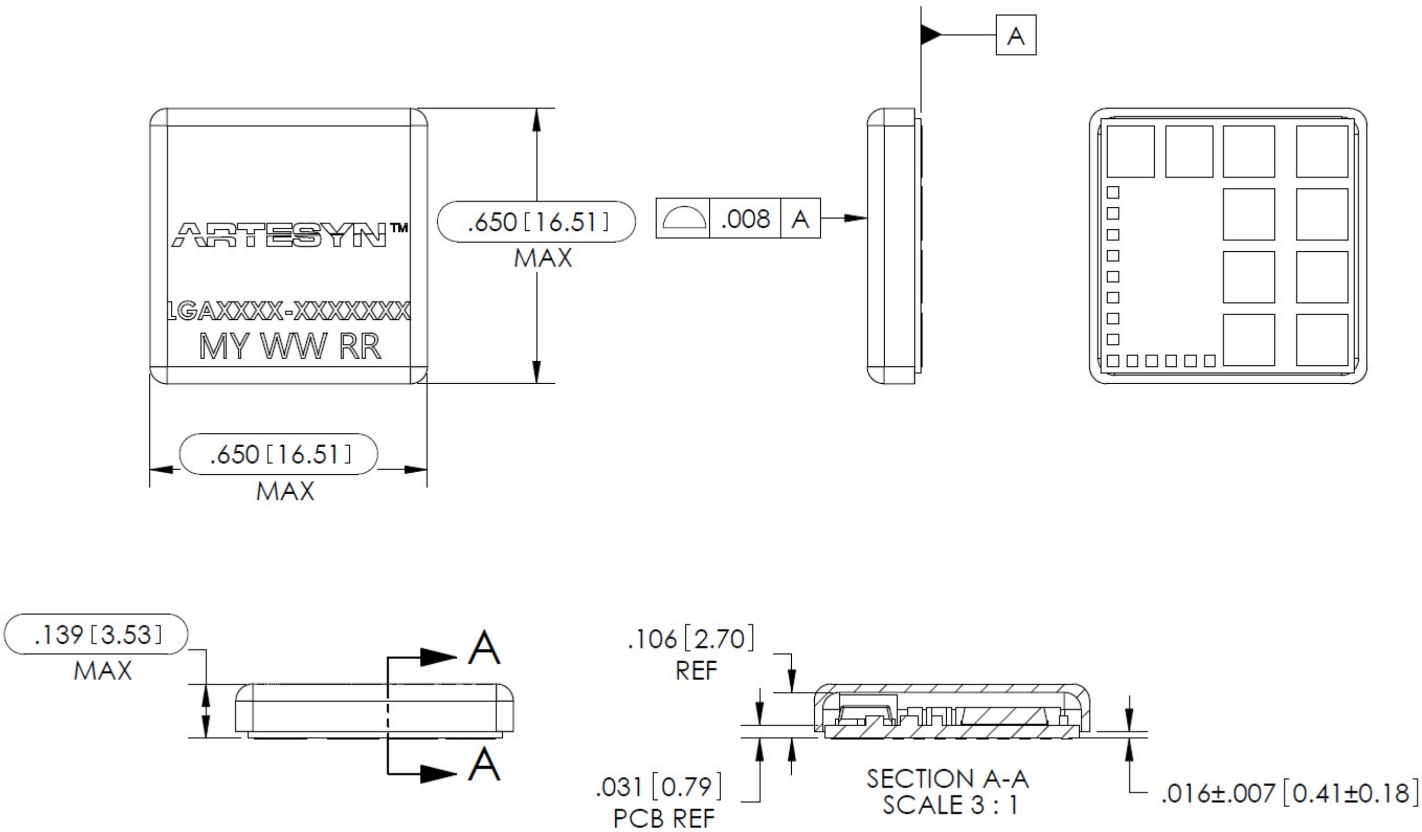
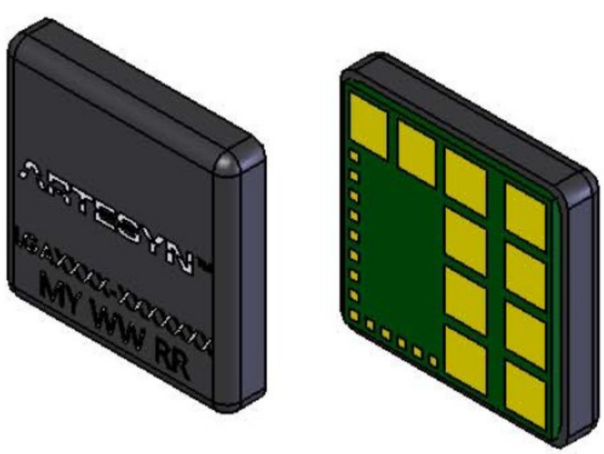


Table 4. Component Height:

Model #	DIM A in (mm)
LGA03	0.129 (3.27)
LGA06	0.129 (3.27)
LGA10	0.129 (3.27)
LGA20	0.210 (5.33)



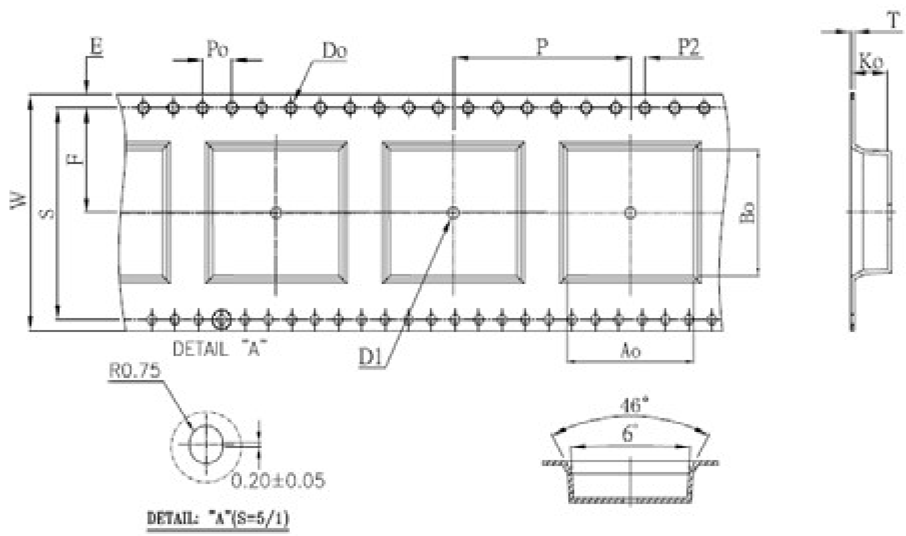
Notes: Dimensions are in inches and (millimeters)
Tolerance: ±0.010in (±0.25mm)

Pin Assignment

Pin No.	Name	Pin No.	Name
1	Vout	13	+Offset
2	Vout	14	-Sense
3	Vout	15	+Sense
4	Vout	16	NC
5	GND	17	NC
6	GND	18	NC
7	GND	19	NC
8	GND	20	NC
9	Vin	21	Enable
10	Vin	22	Power Good
11	NC	23	Margin Control
12	-Offset	24	Trim

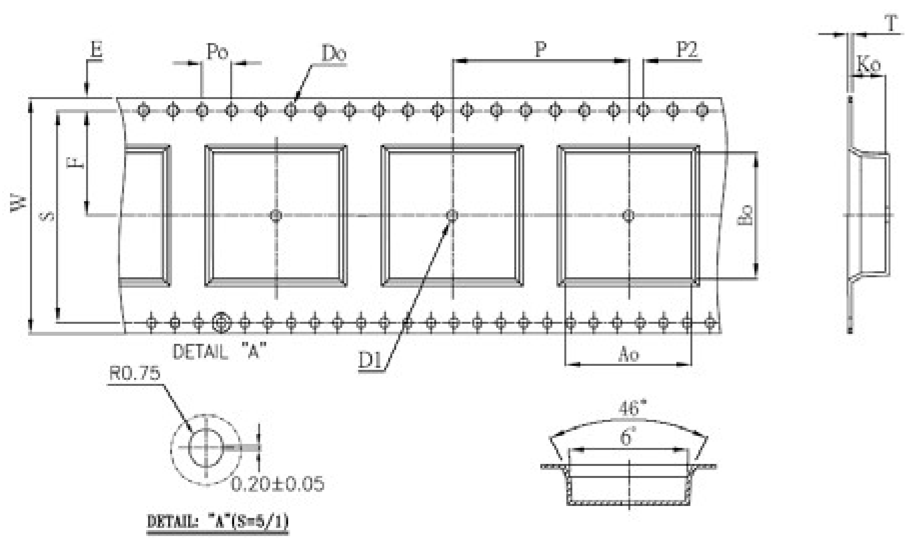
Packing

LGA03C, 06C, 10C



EIA Dimensions (mm)	
W	32.0 ±0.30
E	1.75 ±0.10
F	14.2 ±0.10
So	28.4 ±0.10
P	24.0 ±0.10
Po	4.0 ±0.10
P2	2.0 ±0.10
Do	Ø 1.5 +0.10 -0.00
D1	Ø 2.0 MIN
T	0.40 ±0.05
Ao	16.6 ±0.10
Bo	16.7 ±0.10
Ko	3.7 ±0.10

LGA20C

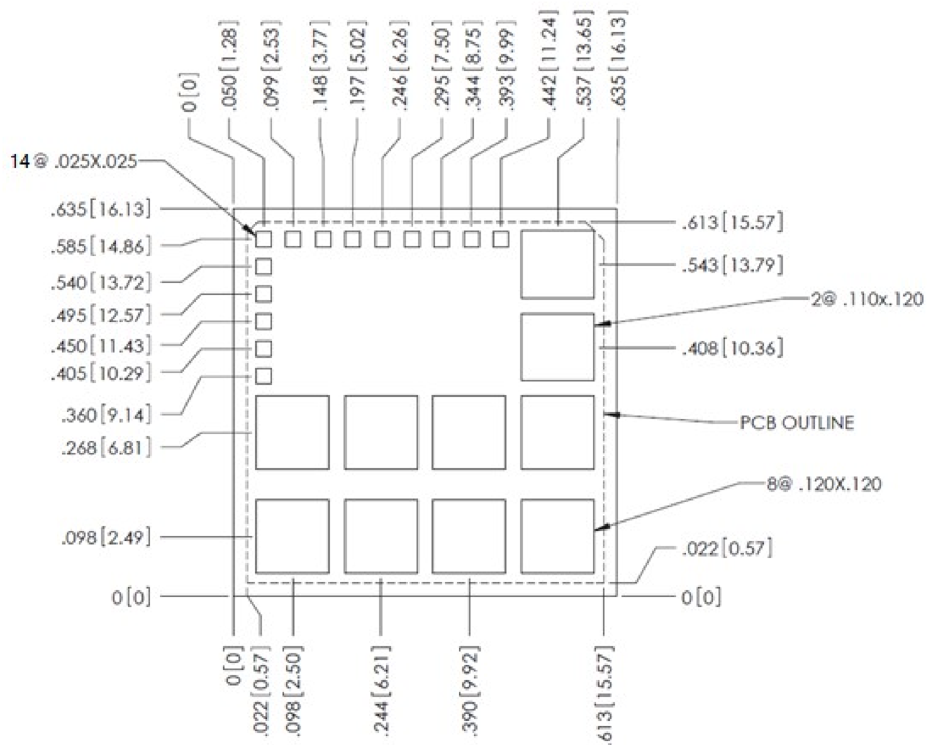


EIA Dimensions (mm)	
W	32.0 ±0.30
E	1.75 ±0.10
F	14.2 ±0.10
So	28.4 ±0.10
P	24.0 ±0.10
Po	4.0 ±0.10
P2	2.0 ±0.10
Do	Ø 1.5 +0.10 -0.00
D1	Ø 2.0 MIN
T	0.40 ±0.05
Ao	16.8 ±0.10
Bo	16.8 ±0.10
Ko	5.8 ±0.10

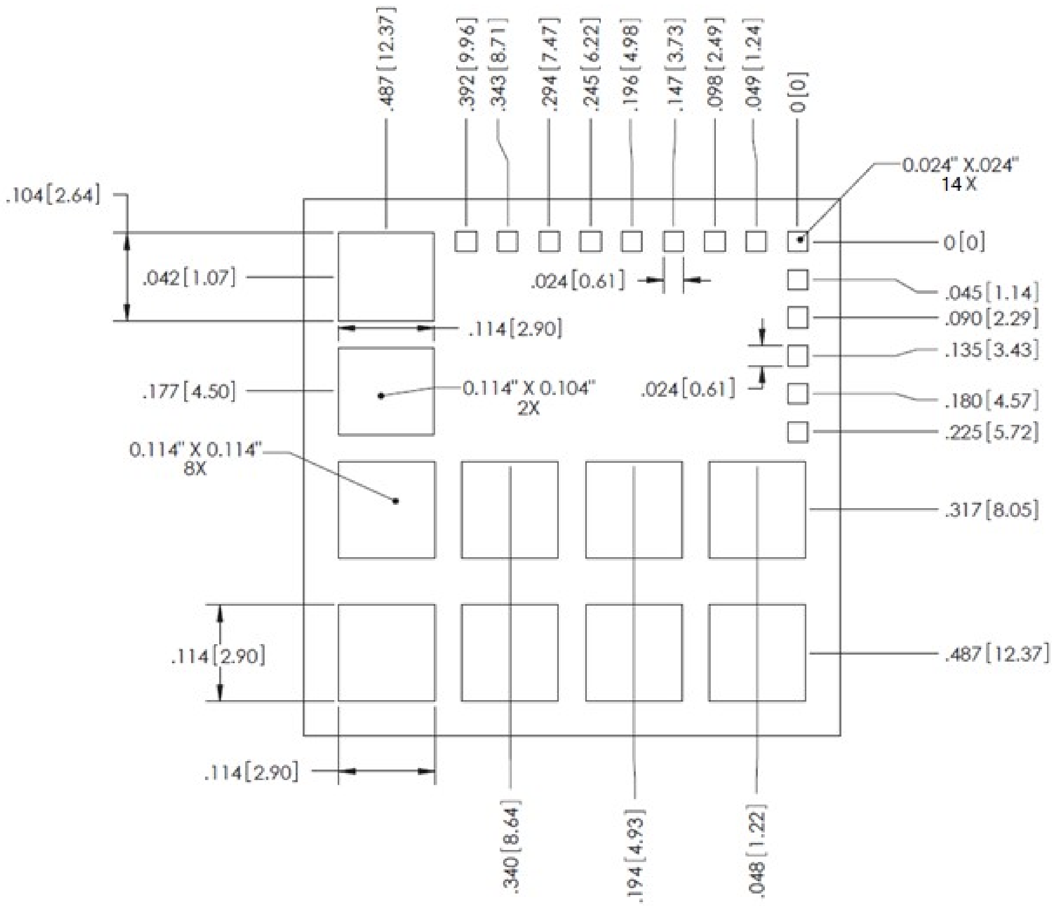
Note 1 - T&R packaging comes in Standard 13" reel size.
Note 2 - Tape material: Black, Anti-static Polystyrene Amine free.
Note 3 - Surface Resistivity: <1012 Ohms/Sq
Note 4 - Module quantity/reel: LGA03C, LGA06C, LGA10 C = 600 pcs
LGA20C = 450pcs.

Recommended Application

System Board Footprint



Solder Paste Stencil



Note: The stencil thickness for soldering module to load board is recommended as 6mil. (see window paning on page 29)

Application Notes

Electrical Description

The LGA C Series is implemented using a voltage mode single-phase synchronous buck topology. A block diagram of the converter is shown in Figure 44.

The output voltage is adjustable over a range of 0.59 - 5.1V by using a resistor or voltage as described on Page 25. (Factory preset is 0.591V.)

The converter can be shut down via the remote ON/OFF. The remote ON/OFF operates with positive logic that is compatible with popular logic devices. Positive logic implies that the converter is enabled if the remote ON/OFF input is high (or floating), and disabled if it is low.

The power good signal is an open collector output that is pulled low by the PWM controller when it detects the output is not within ±10% of its set value.

The output is monitored for overcurrent and short-circuit conditions. When the PWM controller detects an overcurrent condition, it forces the module into hiccup mode.

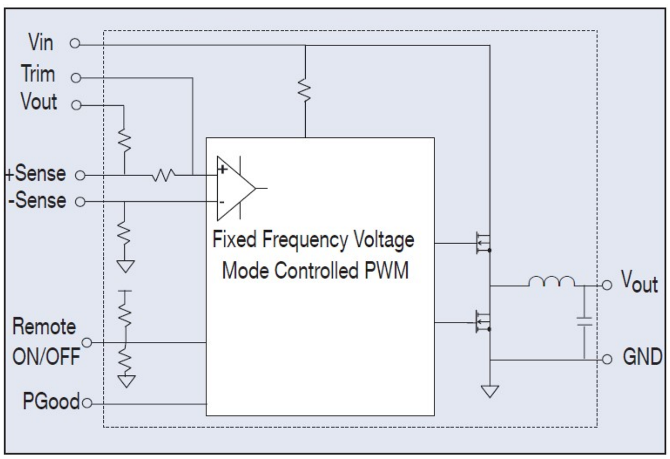


Figure 44: Electrical Block Diagram

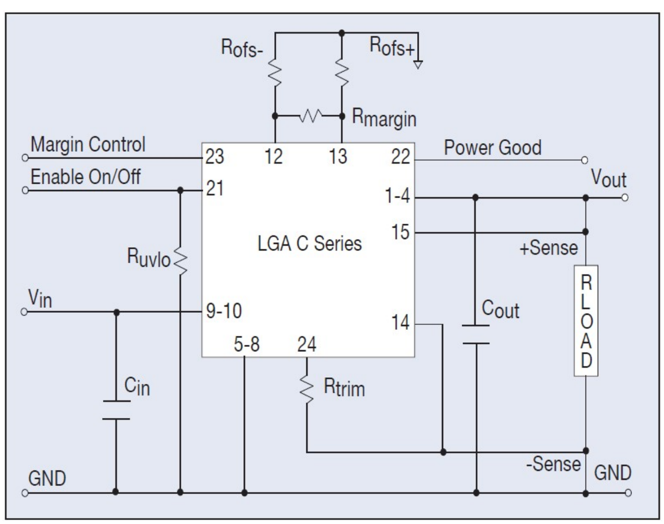


Figure 45: Standard Application Drawing

Wide Operating Temperature Range

The LGA C series's ability to accommodate a wide range of ambient temperatures is the result of its extremely high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal performance of the thermally enhanced cover. The maximum output power that the module delivers will depend on a number of parameters, primarily:

- Input voltage range
- Output load current
- Air velocity (forced or natural convection)
- Addition of heatsink

The LGA C Series module has an operating temperature range of -40 ^{O}C to 85 ^{O}C with suitable derating.

Remote ON/OFF

The remote ON/OFF input allows external circuitry to put the LGA C Series converter into a low dissipation sleep mode. Positive logic remote ON/OFF is available as standard.

The EPD is turned on if the remote ON/OFF pin is high or floating. Pulling the pin low will turn off the EPD. To guarantee turn-on, the enable voltage must be above 0.50V. To turn off the enable voltage, it must be pulled below 0.2V.

Figures illustrating the response of the unit to switching on and off using the remote ON/OFF feature are included in the performance curves on pages 8, 10, 12 and 15. Figures 46 and 47 show various circuits for driving the remote ON/OFF feature. The remote ON/OFF input can be driven through a discrete device (e.g. a bipolar signal transistor) or directly from a logic gate output. The output of the logic gate may be an open-collector (or open-drain) device. Please note the remote ON/OFF pin should only be driven in the following range:

If, Vin ≤ 5V, Von/off (max) = Vin
If, Vin > 5V, Von/off (max) = 5V

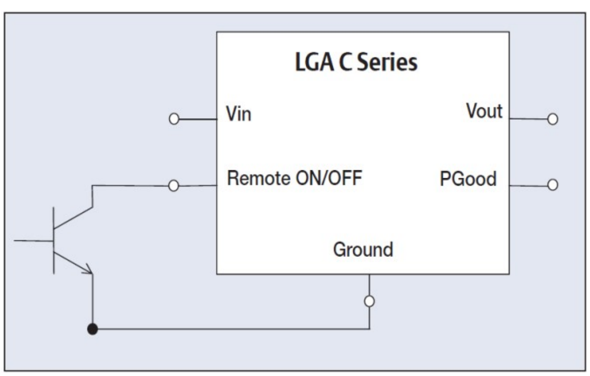


Figure 46: Remote ON/OFF Input Drive Circuit for Non-Isolated Bipolar

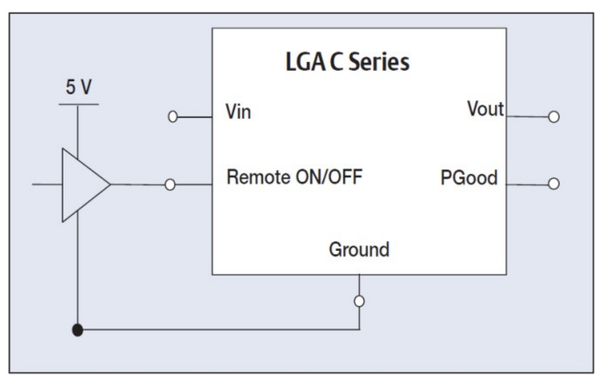


Figure 47: Remote ON/OFF Input Drive Circuit for Logic Driver

Output Voltage Adjustment

The output voltage of the module can be adjusted from 0.59V to 5.1V. This is accomplished by connecting an external resistor between Trim and -Sense as shown in Figure 48 and graphed in Figure 51 or by driving the Trim pin with an external voltage as shown in Figure 49. High accuracy setpoints can be achieved with the use of a potentiometer as shown in Figure 50.

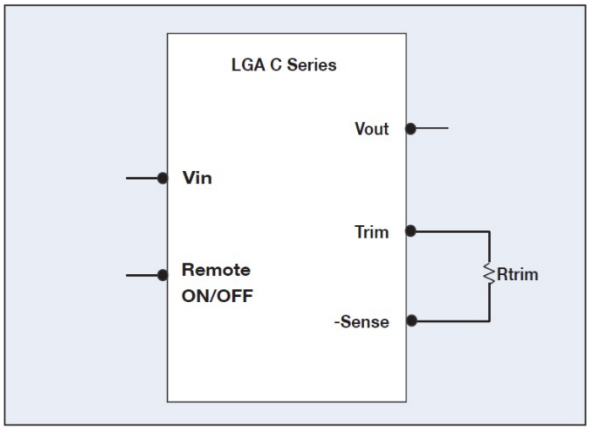


Figure 48: Output Voltage Trim

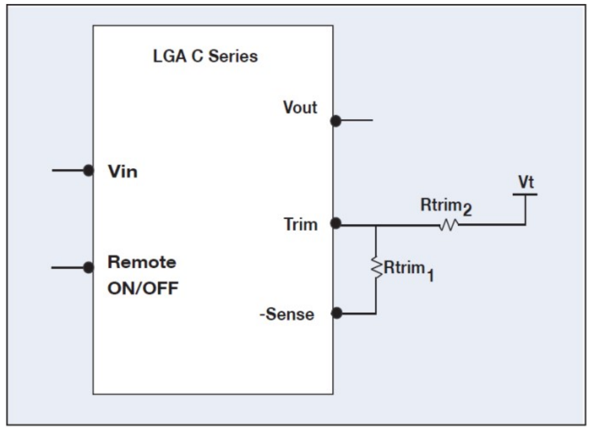


Figure 49: Voltage Trim - with Voltage Source

The trim equation for the basic configuration shown in Figure 48 is:

$$R_{trim} = \frac{1.182}{V_{out} - 0.591}(K\Omega)$$

Where V_{out} is the desired output voltage and R_{trim} is the resistance required between the Trim pin and -Sense.

The trim equation for the external voltage configuration shown in Figure 49 is:

$$R_{trim2} = \frac{R_{trim1}(1.182 - 2Vt)}{R_{trim1}(V_{out} - 0.591) - 1.182}(K\Omega)$$

Where V_{out} is the desired output voltage, R_{trim1} (kΩ) and R_{trim2} (kΩ) are the resistors in Figure 49 and Vt is the applied external output voltage.

Note: If, Vin ≤ 5V, Vpin24 (max) = Vin

If, Vin > 5V, Vpin24 (max) = 5V

The trim equation for the potentiometer configuration show in Figure 50.

$$V_{out} = \frac{0.591}{(R_{trim2} + R_{pot})R_{trim1}} * (2R_{trim2} + 2R_{pot} + R_{trim1}R_{trim2} + R_{trim1}R_{pot} + 2R_{trim1})$$

Where V_{out} is the desired output voltage, R_{trim1} (kΩ) and R_{trim2} (kΩ) are the resistors in Figure 50 and R_{pot} is the resistance of the potentiometer.

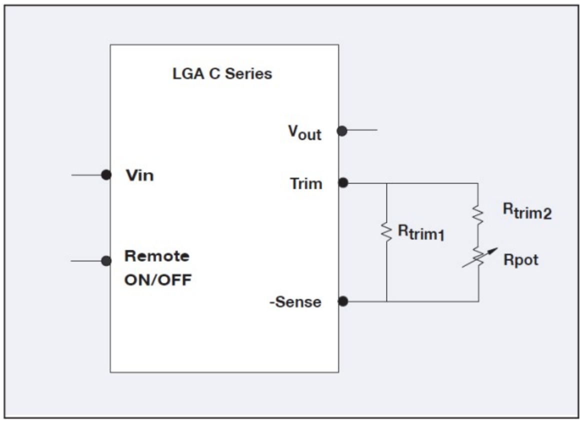


Figure 50: Output Voltage Trim - with Potentiometer

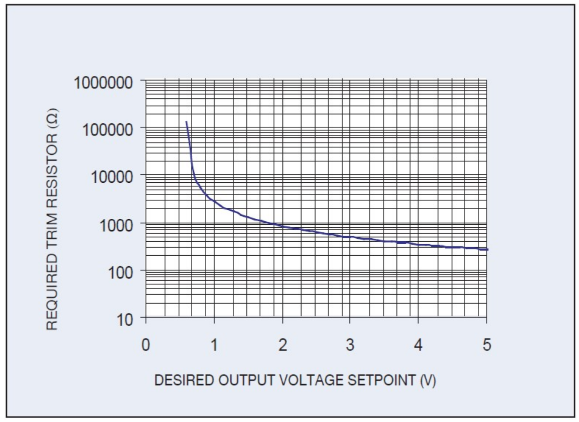


Figure 51: Typical Trim Curves

Power Good

The LGA C modules have a power good indicator output. This output pin uses positive logic and is open-collector. Also, the power good output is able to sink 10mA.

When the output of the module is within ±10% of the nominal set point, the Power Good pin can be pulled high. Note that Power Good should not be pulled higher than the following conditions:

If, Vin ≤ 5V, Vpgood (max) = Vin

If, Vin > 5V, Vpgood (max) = 5V

Current Sink Capabilities

The LGA C series of dc-dc converters is able to current sink as well as current source. The EPD operates over the full output current range at any specified output voltage. This feature allows the LGA C to fit into any voltage termination application.

Output Capacitance

The LGA C Series has output capacitors inside the converter. Limited output capacitance, 10uF for the 3A/6A/10A and 50uF for the 20A, is required for stable operation. When powering loads with large dynamic current requirements, improved voltage regulation is obtained by inserting low ESR capacitors as close as possible to the load. Low ESR ceramic capacitors will handle the short duration high frequency components of the dynamic current requirement. In addition, higher values of electrolytic capacitors should be used to handle the mid-frequency components.

It is equally important to use good design practices when configuring the dc distribution system. Low resistance and low inductance PCB layout traces should be utilized, particularly in the high current output section. Remember that the capacitance of the distribution system and the associated ESR are within the feedback loop of the power capabilities, thus affecting the stability and dynamic response of the module.

Note that the maximum rated value of output capacitance varies between models and for each output voltage setpoint. A stability vs. Load Capacitance calculator, (see your sales representative), details how an external load capacitance influences the gain and phase margins of the LGA C Series modules.

Setting Margin Control

To margin the output voltage up, pull the margin control pin high. To margin down, pull the margin control pin low. If the pin is left floating, the feature is disabled. The maximum margining range is ±33% of the output default voltage setting, with maximum output at 5.5V. The equations for margining up and down are as follows:

$$V_{margin\_up} = 0.1182 * \frac{R_{margin}}{R_{ofs+}} * \frac{R_{trim} + 2k}{R_{trim}}$$

$$V_{margin\_down} = 0.1182 * \frac{R_{margin}}{R_{ofs-}} * \frac{R_{trim} + 2k}{R_{trim}}$$

Note: The margin control pin cannot be pulled in the following range:

If, Vin ≤ 5V then V_{margin}(max) = Vin

If, Vin > 5V then V_{margin}(max) = 5V

See Table 5 for suggested margining values.

Table 5. Suggested Margin Values:

Margin Up and Down 5%								
V_{out_nom} (V)	R_{trim} (kΩ)	R_{margin} (kΩ)	R_{ofs-} (kΩ)	R_{ofs+} (kΩ)	V_{margin_down} (V)	V_{out_down} (V)	V_{margin_up} (V)	V_{out_up} (V)
0.9	3.83	2.49	10.0	10.0	0.045	0.855	0.045	0.945
1.2	1.96	2.49	10.0	10.0	0.059	1.141	0.059	1.259
1.8	0.976	2.49	10.0	10.0	0.090	1.710	0.090	1.890
2.5	0.619	2.49	10.0	10.0	0.125	2.375	0.125	2.625
3.3	0.432	2.49	10.0	10.0	0.166	3.134	0.166	3.466
5.0	0.267	2.49	10.0	10.0	0.250	4.750	0.250	5.250
Margin Up and Down 10%								
0.9	3.83	4.99	10.0	10.0	0.090	0.810	0.090	0.990
1.2	1.96	4.99	10.0	10.0	0.119	1.081	0.199	1.319
1.8	0.976	4.99	10.0	10.0	0.180	1.620	0.180	1.980
2.5	0.619	4.99	10.0	10.0	0.250	2.250	0.250	2.750
3.3	0.432	4.99	10.0	10.0	0.332	2.968	0.332	3.632
5.0	0.267	4.99	10.0	10.0	0.501	4.499	0.501	5.501

Reflow Guidelines

For a SnPb process: pads should be above 183 ^{O}C (liquidus) for 90 seconds max (60-75 seconds typical) with a peak temperature of 225 ^{O}C. For a lead-free SAC305 process: pads should be above 217 ^{O}C (liquidus) for 90 seconds max (60-75 seconds typical) with a peak temperature of 250 ^{O}C.

The LGA Series products passed solderability testing per J-STD-002B and IEC-60068-2-58. The test was conducted by Process Sciences, Inc in August, 2007.

Water Washing

Water-washing is not recommended.

Interface Finish

Electroless Nickel Immersion Gold (ENIG).

Solder Paste

Solderballs are caused between LGA and substrate due to printing an excessive amount of solderpaste. Stencil apertures should be windowpaned; dividing them into quadrants rather than printing a continuous deposit over the entire pad. This will control the amount of solder available to form a joint between LGA and customer board. Additionally, this will also reduce the formation of voids.

Solder Paste Window Paning

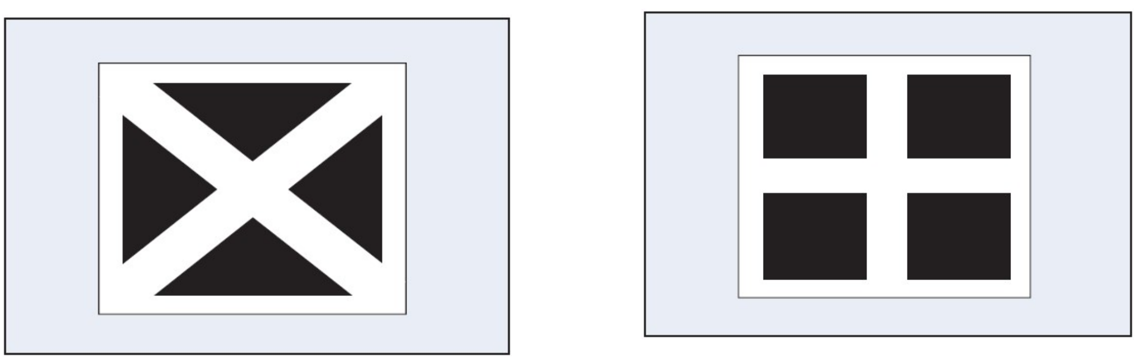


Figure 52: Window Paning

Thermal Hotspot

The electrical operating conditions of the LGA (shown below) determine how much power is dissipated within the converter.

- Input voltage (Vin)
- Output voltage (Vo)
- Output current (Io)

The following parameters further influence the thermal stresses experienced by the converter:

- Ambient temperature
- Air velocity
- Thermal efficiency of the end system application
- Parts mounted on system PCB that may block airflow
- Real airflow characteristics at the converter location

In order to simplify the thermal design, a number of thermal derating plots are provided in this Technical Reference Note. These derating graphs show the load current of the LGA versus the ambient air temperature and forced air velocity. However, since the thermal performance is heavily dependent upon the final system application, the user needs to ensure the thermal reference point temperatures are kept within the recommended temperature rating. It is recommended that the thermal reference point temperatures are measured using a thermocouple or an IR camera. In order to comply with stringent Artesyn Embedded Technologies derating criteria the ambient temperature should never exceed 85 ^{O}C. The case maximum recommended temperature is 100 ^{O}C. Please contact Artesyn for further support.

Figure 53: Thermal Hotspots
1: With Heatsink
2: Without Heatsink

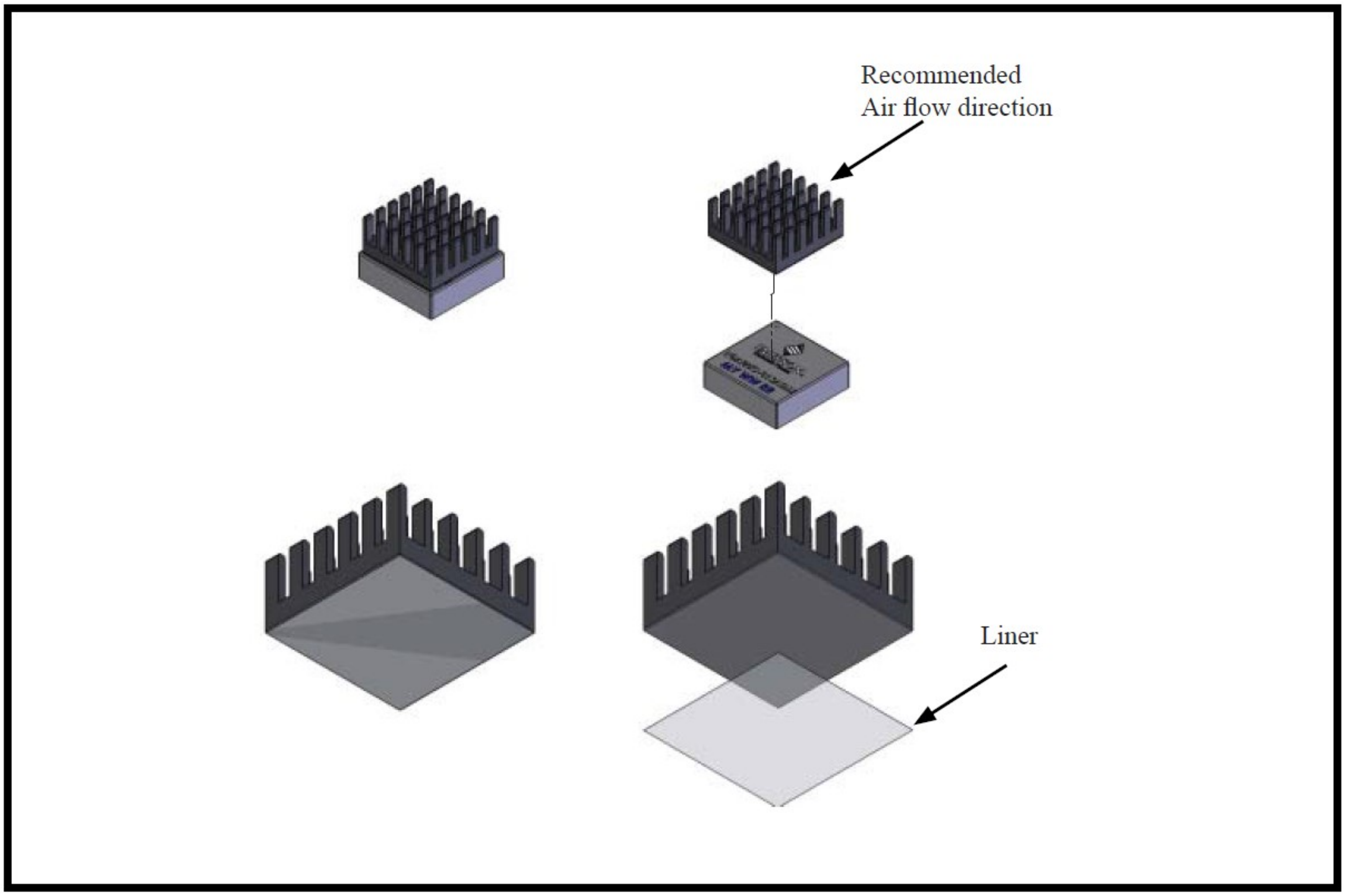
Heatsink Accessory

System should be reflowed before attaching heatsink.

Clean the top surface of the case with isopropyl alcohol and ensure the case surface is air-dried.

Remove clear plastic liner from bottom of the heatsink to expose the adhesive.

Align heatsink with case and apply even pressure (10-15 PSI) for 10-20 seconds.



Heatsink Number System with Options:

Product Family		Product		Purpose		Height*
LGA	-	HTSK	-	KIT	-	XXX
Land Grid Array		Heatsink		Heatsink and Adhesive		Total Height (LGA20 + Heatsink) 045 = 0.45" 048 = 0.48" 050 = 0.50"

Note* - Height is the total height of the LGA20C-00SADJJ with heatsink attached.

Record of Revision and Changes

Issue	Date	Description	Originators
1.0	03.20.2018	First Issue	A. Zhang
1.1	12.24.2018	Update the system board footprint	K. Wang